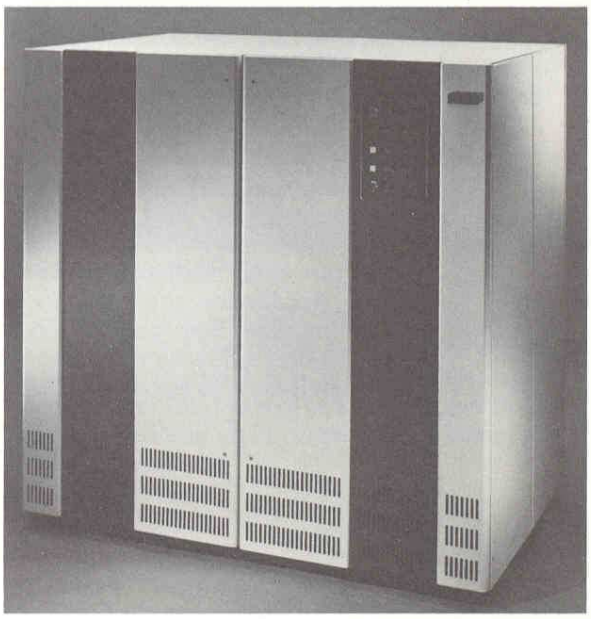
Product Bulletin

PRIME

Prime 9955™

Features

- High performance, 32-bit supermini with up to 16 Mb of error correcting, high-speed MOS memory.
- High-speed, emitter-coupled logic (ECL) circuitry.
- Pipelined central processor organization allowing concurrent processing of up to five instructions.
- 64Kb of high-speed, bipolar cache memory to reduce memory access time.
- One-button system start-up to multi-user level.
- Environmental sensing to detect over-temperature occurrence.
- Up to 254 terminals supported, with up to 255 active processes.
- Hardware implemented instructions for quad precision floating point operations (96-bit).
- Diagnostic Processor with two integrally packaged floppy diskettes for loading of operational and diagnostic microcode.
- Full hardware and software compatibility with all Prime 50 Series™ systems.
- Efficient, multifunctional PRIMOS® operating system, plus a wide range of available system and application software.



Description

The Prime® 9955 superminicomputer is a high-performance, interactive superminicomputer ideal for computational, commercial or CAD/CAM/CAE applications in standalone or distributed environments. Hardware and software compatible with the entire line of Prime 50 Series systems, the high-performance Prime 9955 includes a 32-bit CPU featuring ECL circuitry and pipelined architecture, up to 16 Mb of error-correcting MOS memory, burst-mode I/O, hardware instruction assists, 64Kb cache memory, a sophisticated diagnostic processor and the PRIMOS operating system. The standard system chassis includes optional board positions for memory, any standard peripheral subsystem, asynchronous line controllers, multiline data controller for synchronous communications or the PRIMENET™ Node Controller (PNC), for high-speed local networks.

The Prime 9955 supports up to 254 terminals in an interactive environment of up to 255 processes.

Prime 50 Series Architecture Features

Compatibility

Prime systems are designed for software and hardware compatibility. Like all Prime 50 Series systems, the Prime 9955 uses the PRIMOS operating system. The single operating system ensures total software portability across all Prime systems. User programs developed on one system will run on all others without recompilation. In addition, programmers use the same set of commands on all systems. Software compatibility also promotes the cost effectiveness of using the Prime 9955 as a host processor in a networked environment.

Because the Prime 9955 is I/O compatible with the entire Prime product line, peripheral controllers can be interchanged between different systems for flexibility and cost-effective upgrade and expansion.

32-Bit Architecture

The Prime 9955 computer's 32-bit architecture increases internal operating efficiency for large program support. Full 32-bit word length allows more information to be processed during each machine cycle than is possible with 16-bit systems. In addition, the Prime 9955 can easily accommodate large programs because the 32-bit word length allows a very large number of address locations to be specified.

Virtual Memory Management

Running under the PRIMOS operating system, the Prime 9955 gives each user a virtual address space much larger than physical memory. Each user has 512Mb of virtual address space; 32Mb are reserved for private user program space. The rest is for shared libraries and system functions.

System functions, such as I/O, are embedded in the virtual address space of each process. This design increases system throughput by using ordinary procedure calls, eliminating the overhead of special system calls. A protection ring mechanism ensures operating system integrity.

Program Environment

Prime 9955 programs operate in a multi-segment environment that includes a stack segment containing all local variables, a procedure segment containing executable code and a linkage segment containing statically allocated variables and linkages to common data. In addition, stack management overhead is minimized by implementing the procedure call mechanism in firmware.

Featuring stack management mechanisms, the Prime 9955 optimizes the efficiency of passing, subroutine and procedure calls, arithmetic expression evaluation, and dynamic allocation of temporary storage. These mechanisms also support re-entrant and recursive procedures.

High-Density MOS Memory

Main memory of the Prime 9955, and all Prime processors, features high-density, 64K MOS semiconductors. Prime 9955 memory array boards interface to a memory controller that is considered part of the central processor. The memory controller performs all common timing and error checking and correction functions for the Prime 9955's memory. This allows memory to be packaged in 2 Mb memory array boards, for maximum reliability and space efficiency. Main memory is expandable up to 16Mb on the Prime 9955. For enhanced memory throughput, the Prime 9955 has a 64-bit data path between the central processor and main memory. Because the Prime 9955's 2 Mb memory array boards are self-interleaving, there is no need to have an even number of boards.

Register Sets

Each Prime 9955 has eight register sets, each containing 32 registers for a total of 256 32-bit registers. Four of these register sets are used for the process exchange mechanism. One stores the execution state of the currently active process. The other three contain information about the state of the previously active processes. These four register sets greatly reduce process exchange overhead in multi-user environments.

Three register sets act as microcode scratch registers, further enhancing the processing efficiency of the Prime 9955 CPU. The last register set supports the burst mode input/output transfer mechanism by holding status information about the 32 direct memory access (DMA) channels.

High-Speed Address Buffer

A high-speed buffer called the Segment Table Lookaside Buffer (STLB) stores frequently used virtual-to-physical address translations.

The STLB's large storage capacity on the Prime 9955 is 512 entries. Measurements have shown that 99% of the time, PRIMOS can find the needed physical addresses in the STLB. Access to the STLB is completely overlapped with access to cache for maximum speed.

The Prime 9955 uses an I/O bus mapping scheme to allow I/O bus transfers to come from, or go to, any location in physical memory. This mapping scheme embodies virtual-to-physical address translations. The Prime 9955 has an I/O Translation Lookaside Buffer (IOTLB), with 512 entries that allow mapping translations to occur within the hardware of the CPU.

Protection Rings

A comprehensive hardware-controlled memory protection system has a multiring hierarchy that lets programs be assigned to any of several security levels. This gives many users full access to specified programs and protects other programs and databases from unauthorized access, as well as preventing inadvertent damage to system software.

9955 Special Features

Five-Stage Pipeline Architecture

The five-stage pipeline organization of the Prime 9955 central processor provides overlapped instruction execution, and allows five instructions to be in some stage of execution concurrently. This innovative design permits overlap of cache access, instruction decode, effective address formation, virtual memory mapping and instruction execution.

To support this pipeline, the Prime 9955 has a "branch cache memory" with 1024 entries to keep track of program branches and to predict which way a branch will go. Measured statistics show that the branch cache is more than *80%* successful in ensuring that the pipeline is processing the appropriate instruction, thus benefitting from overlapped instruction execution.

Emitter-Coupled Logic (ECL) Circuitry

The Prime 9955 CPU uses very high-speed ECL circuit technology to achieve a new level of processor performance. These logic circuits are approximately twice as fast as the Transistor-Transistor Logic (TTL) circuits used on the smaller Prime 50 Series systems, thus contributing to the performance advantage of the Prime 9955.

Process Exchange

Like all Prime 50 Series systems, the Prime 9955 uses a high-speed process exchange facility to accelerate performance in a multi-user environment. This facility manages context switching, in which an active process is suspended and a new process is activated. Context switching algorithms are coded in highly-optimized programs for exceptional efficiency.

Process exchange firmware is complemented by hardware. For the Prime 9955, there are four register sets that store the execution state of the currently-active and three previously-active processes.

When the state of the process resides in one of the four parallel register sets, that process can be reactivated in 1.9 microseconds. Even when the execution state of a process must be loaded and stored from memory, processes are exchanged in 7.6 microseconds. This exceptional speed reduces context switching overhead to an absolute minimum, and accelerates performance in all multi-user applications.

Cache Memory

Cache memory greatly reduces effective memory access time by storing frequently-used instructions and data in a fast buffer memory located within the central processor. The high-speed components and efficient circuit configuration provide a cache access time of only 40 nanoseconds. Its 64Kb capacity and greater than 98% hit rate result in an effective main memory access time of only 58 nanoseconds.

Soft Error Recovery

Soft Error Recovery enhances the larger cache memory, STLBs, and IOTLBs of the Prime 9955. When a parity error is detected in either the cache or the lookaside buffers, the CPU will reload that location from main memory. This recovers all soft errors and avoids a halt.

Instruction Set

The Prime 9955 instruction set is designed for speed, efficiency, high-level language execution, and compatibility across all Prime processors.

For maximum performance, the instruction set hardware fully exploits the Prime 9955 supermini's 32-bit internal data paths and registers. Instructions frequently executed by application programs are supported by hardware assists to microcode for accelerated execution speed.

The instruction set is also designed to enhance the run-time efficiency of high-level languages. For example, it provides firmware implementations of such high-level language constructs as string functions (COBOL and PL/I) and the computed GOTO (FORTRAN).

The Prime 9955 instruction set is a compatible superset of the standard Prime 50 Series instruction set. Consequently, user programs written for any Prime system can run on the Prime 9955 without data conversion, or relinking.

I/O Transfer Efficiency

For maximum speed, direct memory access (DMA) data transfers are supported by "burst-mode" transfer mechanisms. Burst-mode I/O transfers 64 bits of data at a time over the Prime 9955 system's 9Mb I/O bus. This 9Mb bandwidth is many times greater than the transfer rate of today's fastest peripheral storage devices, and allows them to attain their maximum level of performance.

Burst-mode transfer also enhances the efficiency of virtual memory management, by increasing the speed at which pages are transferred from disk to main memory.

Loadable Control Storage

Like all other members of the Prime 50 Series, the Prime 9955 has a microprogrammed central processor. Two diskette drives are supplied as an integral part of the Prime 9955. Memory is automatically loaded from one diskette when the Prime 9955 is turned on. The other diskette is used for loading diagnostic microcode. A portion of the diagnostic microcode is automatically loaded into the control store and run during Prime 9955 system startup. Following successful verification of the integrity of the central processor and memory interface, the operational microcode replaces the diagnostic microcode in the control store. Should verification fail, the Prime Customer Service Representative can run a second level of diagnostic microcode that is very extensive and will overlay the control store up to 6 times. This will pinpoint any problem to a specific area of the central processor and/or memory interface.

Multiplier Array

The Prime 9955 features a multiplier array that enables it to multiply in less than half the time required by any previous Prime 50 Series system. The new multiplier array is 8 by 48 bits, and utilizes the MECL Macrocell array.

Quad-Precision Floating Point

A major instruction set feature on the Prime 9955 is quad-precision floating point. In this format, the fraction (mantissa) has been expanded to 96 bits from the 48 bits available with double-precision floating point. The mantissa and the exponent are manipulated in parallel by the floating point logic to reduce execution time. The extra accuracy of quad-precision floating point is valuable in certain scientific and mathematical applications that need extra digits of precision. Prime's FORTRAN compiler (F77) has been enhanced to support quad-precision floating point. However, any Prime 50 Series system can emulate quad-precision floating point by automatic invocation of software routines. This preserves program compatibility between the Prime 9955 and other Prime 50 Series systems.

Diagnostic Processor

The Prime 9955 diagnostic processor performs a variety of system integrity, administrative and monitoring functions. The diagnostic processor controls the two floppy disks used to load operational and diagnostic microcode. The system Status Panel, with operator switches and indicators, interfaces to the diagnostic processor, as does the operator's console.

The diagnostic processor also controls an automatic system startup feature, which results in the Prime 9955 going from a no-power condition to multi-user PRIMOS. Time of day and date are fed to PRIMOS, at the appropriate point, from a battery-operated clock on the diagnostic processor, which is trickle-charged when the Prime 9955 is running. The clock will keep time for up to one month when the Prime 9955 has no power.

Environmental Sensing

By monitoring the system airflow and temperature sensors, the diagnostic processor can detect problems with the computer room air conditioner or an internal Prime 9955 cooling problem. The PRIMOS operating system then notifies the operator of any malfunctions.

Local and Remote Diagnostics

The Prime 9955 diagnostic processor can also perform local and remote diagnostics. This provides fast, effective trouble-shooting for identifying a hardware problem and for performing comprehensive system diagnosis.

The local system operator or administrator initiates remote access by depressing a "Remote Enable" button on the control panel. A second button places the remote terminal in monitoring mode and allows it to control the system as if it were the local system console. When the system is in control mode, a Customer Service Representative can run the system completely from a remote terminal, including such tasks as bootloading and on-line operations.

Two indicators display the state of the remote communications link: one indicates that a remote user has been given the ability to dial into the system and monitor operations; the second indicates whether a remote access is in progress and flashes when the remote user has been given control of the system.

Software

The PRIMOS operating system supports both interactive and batch processing on all Prime 50 Series systems. The operating system supports re-entrant procedures, letting many users share a single copy of a software module.

A wide range of high-level, industry-standard languages run on Prime systems. Available languages include FORTRAN 77, ANSI 74 COBOL, Pascal, PL/I Subset G, C, BASIC and RPG II. The Prime Macro Assembler, the Source-Level Debugger, and EMACS, the extendable screen editor, support these standard languages.

Prime offers a comprehensive family of data management products. Central to these are MIDASPLUS™ and PRISAM™ indexed sequential access managers, and CODASYL-compliant Prime DBMS. Complementing these data managers are: FORMS for screen management, PRIME/POWER + for query and reporting on MIDASPLUS and PRIMOS files, and DISCOVER™ for query and reporting on PRISAM and Prime DBMS files.

Other Prime software offerings include PRIMEWAY™ Development and Transaction Management System, Prime INFORMATION,™ a fourth generation, relationally-based data management environment, and Prime's Office Automation System (OAS).

For CAD/CAM/CAE applications, Prime offers the Prime MEDUSA™ Mechanical Engineering design package; the Product Design Graphics System™ (PDGS)™; and the SAMMIE ergonomic design software packages. In addition, a large library of application packages is available from the Prime Users Library Service (PULSE) and from the Joint Marketing Agreements (JMA) that we have with third-party software houses.

Networking

The Prime 9955 is ideal for networking and distributed processing environments. PRIMENET networking software lets Prime computers communicate among themselves, with terminals, and with other manufacturers' systems. Using PRIMENET facilities, users can remotely log into other systems, share files among systems, and develop distributed applications. For local area networks, the Prime 9955 can be attached in a high-speed RINGNET™ network with any other Prime 50 Series system. The ring provides intersystem communication via a coaxial cable or fiber optics for Prime systems using PRIMENET software and a PRIMENET node controller.

The Prime 9955 supports all Prime communications hardware controllers. Available hardware options include IBM BISYNC for HASP and 2780/3780; High-Level Data Link Control (HLDC) protocol for X.25 packet-switching networks; Control Data 200UT; UNIVAC 1004; Honeywell GRTS; ICL 7020; and XBM.

Prime's Distributed Processing Terminal Executive (DPTX) lets the Prime 9955 emulate and support 3271/3277 Display Systems.

The Prime/SNA™ product family allows Prime systems to coexist with networks based on IBM's system network architecture, SNA.

Peripherals

The Prime 9955 supports a wide range of peripheral products for mass storage, data entry and retrieval, communications and hardcopy output. Peripherals are compatible across the Prime product line for easy, economical system upgrade.

Up to 10 billion bytes of data can be stored on line using Storage Module Disk or Fixed Media Disk subsystems. Magnetic tape products include a 75 ips, 6250 bpi GCR unit and a streaming tape subsystem, with up to eight tape drives available per system. The Prime 9955 can support 254 terminals for local and remote input. Printer options available include a wide range of line printers with speed up to 1000 lines per minute, a matrix line printer/plotter and a letter-quality printer.

Regulations and Power

The Prime 9955 has been certified to meet U.S. Safety and Noise Emissions Regulations – U.L. and FCC EMI – as well as Canadian safety regulations. The system can be configured for North American and European A.C. Power Sources.

Specifications

System

Main Memory:	Up to 16Mb
Cache Memory:	64Kb
Effective Memory Access Time:	58 Nanoseconds
Virtual Address Space:	512Mb
Terminals Supported:	Up to 254
Disk Storage:	Up to 10 gigabytes

Physical

Height: 53 inches (135 cm)
Width: 53 inches (135 cm)
Depth: 35 inches (89 cm)

Environmental

Operating Temperature:	59-80°F (10-30°C)
Operating Humidity:	10-80% (non-condensing)
Operating Altitude:	0-12000 ft (0-3.5 Km)
Heat Dissipation:	13,300 BTU's

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