Product Bulletin

PRIME

Prime 850 System

Features

- Integrated multi-stream architecture with parallel instruction stream processing.
- Total compatibility with all 50 Series software and peripherals.
- Error-correcting MOS main memory, expandable from 2Mb to 8Mb.
- Ultra-high MOS memory storage density of 64 kilobits per chip allowing one million-bytes of storage on a single memory board.
- 32Kb bipolar cache memory with 80 nanosecond access time.
- Instruction Preprocessor Units for sequential instruction queuing.
- Hardware-implemented instruction set for floating point arithmetic, decimal arithmetic, and character string operations.
- Burst-mode I/O for high data transfer rate.
- 32-bit architecture with 64-bit interleaved memory data transfer.
- 512Mb virtual address space per user with 32Mb user program address space.
- Simultaneous support of 128 terminals and active user processes.
- PRIMOS® operating system with both interactive and batch mode support.
- Programming language support, including FORTRAN, COBOL, PL/I, Pascal, BASIC, and RPG/II.
- Data management software support, including DBMS (CODASYL compliant), Prime/TAPS, MIDAS, FORMS, and POWER.
- Virtual Control Panel for comprehensive remote system diagnostics capabilities.

Description

The Prime 850 is an integrated system of hardware, firmware, and software. The top-of-the-line system in the Prime 50 Series family, the 850 offers exceptional throughput in an interactive, multi-user, multi-functional environment. Featured on the system is an innovative multi-stream architecture that allows two instruction streams to be processed in parallel. Central to the Prime 850 are two high speed cache memories, 64-kilobit per chip RAM storage, two Instruction Preprocessor Units for sequential instruction queuing, Burst-Mode I/O for 64-bit data transfer, and hardware instructions for floating point arithmetic, decimal arithmetic and character string operations. The Prime 850 is supported by the PRIMOS operating system, ensuring total compatibility with all Prime 50 Series systems, and supports up to 128 active user processes.

Due to the Prime 850's multi-stream architecture, a significant increase in system throughput is achieved. Two different instruction streams can be processed at the same time. Parallel stream processing is managed by the PRIMOS operating system for maximum system efficiency. Main memory is shared by both streams to dynamically fulfill demands on memory requirements. With two instruction streams, the Prime 850 can execute more instructions in environments where users make heavy demands on instruction execution resources.

The Prime 850 is Prime's first system to use ultra-high density MOS chips with 64-kilobit RAM (Random Access Memory) storage. Each memory board provides 1 Mb storage for space and power efficiency.

Supporting the Prime 850 is PRIMOS, the multi-user operating system. PRIMOS is designed to provide each user with maximum system resources on demand. Both instruction streams are managed by the operating system for maximum efficiency.

The Prime 850 high performance, multi-stream system offers increased system throughput, high speed, and low overhead. Ideally suited for use in distributed processing or networking, the Prime 850 system excels in scientific, business and office automation applications.

Multi-Stream Processor Design

The Prime 850 is an innovative implementation of parallel instruction stream architecture. In keeping with Prime's long-standing commitment to "software first" engineering, the Prime 850 is designed to provide maximum hardware support for the timesharing capabilities of PRIMOS. It is an integrated system of software, firmware, and hardware that provides exceptional throughput in multi-user, multi-functional environments.

The Prime 850 simultaneously executes two independent instruction streams under the control of a single embedded operating system. The system consists of two parallel Instruction Stream Units (ISU) that access the same main memory through a common memory bus. Each ISU is made up of an Instruction Preprocessor Unit, an Instruction Execution Unit, and a Cache Memory Unit. The Instruction Preprocessor Unit prefetches instructions from cache memory, decodes instructions, resolves effective addresses, and maintains a sequential instruction queue. The Instruction Execution Unit consists of a floating point Arithmetic Logic Unit (ALU), decimal ALU, integer ALU, and Execution Control Unit. The Cache Memory Unit stores frequently used data and instructions in fast bipolar storage devices for rapid access and greatly reduced memory overhead. A Stream Synchronization Unit protects both ISU's from invalid cache references.

The multi-stream Prime 850 supports up to 128 different user processes. New processes are activated by the Process Exchange facility located in the Execution Control Unit of each ISU. The Process Exchange facility uses firmware instructions for context switching. New processes are automatically introduced to either ISU in less than 35 microseconds for an absolute minimum of scheduling overhead.

Prime's 850 multi-stream architecture is totally user transparent. The PRIMOS operating system automatically manages all system resources for maximum efficiency. It exploits the Prime 850 parallel stream configuration to support an exceptional level of throughput in multi-user environments.

Special Performance Features

Bipolar Cache Memory

The Prime 850 uses cache memory to store frequently used data and instructions for rapid access. Each parallel Instruction Stream Unit contains one 16Kb Cache Memory Unit for a system total of 32Kb cache storage. Cache memory is implemented in high-speed bipolar devices and has a memory access time of only 80 nanoseconds. This large cache storage capacity provides an exceptionally high hit rate of 95%. In each ISU, cache memory is accessed by both the Instruction Preprocessor Unit and Instruction Execution Unit for minimal main memory overhead. Memory mapping is completely overlapped with cache memory to further accelerate system performance. A Stream Synchronization Unit protects both Cache Memory Units from any invalid cache references.

Instruction Preprocessor Unit

Each Instruction Stream Unit has one Instruction Preprocessor Unit for sequential instruction queuing. The Instruction Preprocessor Unit improves central processor performance by prefetching and decoding four instructions ahead of the program counter from cache memory. It accesses cache independently, so the next four instructions are prefetched, decoded and the effective address formed in parallel with instruction execution. When the processor's execution unit is ready for the next sequential instruction, it has been prepared in advance. This results in the Prime 850 spending more time executing and less time in preprocessing and decoding overhead.

Central logic in the Instruction Preprocessor Unit continuously prefetches data from cache to keep the four instruction buffers full. In addition, the Instruction Preprocessor Unit can resolve most indirect addresses, further increasing instruction execution speed.

Bust-Mode I/O

The Prime 850 uses Burst-Mode I/O to increase system throughput by reducing input-output overhead, and maximizing the performance of high-speed peripheral devices. Burst-Mode I/O provides a high-speed transfer rate of 8Mb per second, and transfers 64-bits of data per burst request.

Hardware-Implemented Instructions

The Prime 850 uses hardware-implemented instructions for floating point arithmetic, decimal arithmetic, and character string operations. Hardware instruction support greatly accelerates execution performance in scientific, business, and systems programming applications.

Floating-Point Arithmetic

The Prime 850's 32-bit internal architecture uses hardware-implemented instructions for single and double precision floating point arithmetic. With a 32-bit path between the unit and central processor, the floating-point unit accepts data at an extremely fast rate. Registers assigned to floating point operations are integral to the unit itself, and its use of parallel logic permits exponential and fractional calculations to be done simultaneously. Separate parallel logic performs binary multiplication four bits at a time, division three bits at a time, and addition 48-bits at a time.

Decimal Arithmetic

Decimal arithmetic instructions are implemented in hardware for execution efficiency in business environments. COBOL and PL/I decimal arithmetic operations support up to 18-digit packed or unpacked signed numbers. Operands that differ in data type and/or scale factor are handled automatically during add, subtract, multiply, divide and comparison operations. Hardware instructions also support rounding on numeric operations, and efficient binary-to-decimal and decimal-to-binary conversions.

Character String Operation

Hardware-implemented instructions for character string operations are used to speed execution in business and systems programming environments. Character manipulation is performed on field sizes of virtually any length. Justification, truncation, and padding are automatic in move, compare, translate, edit and similar operations. Numeric and character editing instructions let the user easily produce fields in COBOL and PL/I picture-like formats. For maximum efficiency, all character string operations involve a limited number of in-line instructions.

Basic Architecture Features

Compatibility

The Prime 850 is supported by the PRIMOS operating system, like all other 50 Series systems. A single operating system ensures total software portability across all Prime systems. User programs developed on one system can be executed on any other system without data modifications or source recompilation. Application software can be used with a familiar set of system commands for maximum user productivity. System-wide compatibility also promotes economy when systems need to be upgraded or expanded to meet increasing computer resource demands.

32-Bit Architecture

The Prime 850 uses 32-bit architecture for internal operating efficiency and large program support. Full 32-bit word length allows more information to be processed during each machine cycle than is possible with 16-bit architecture. As a result, the system can do more work per cycle because it is manipulating a larger amount of data. In addition, 32-bit word length allows for the specification of a very large number of memory address locations. Users can run large programs without any need to compromise program design because of address space restrictions. Scientific and engineering applications further benefit from the superior numerical precision capabilities of 32-bit architecture.

Virtual Memory Management

PRIMOS operating system uses efficient virtual memory management to give each user a virtual address space far greater than physical memory. Each user is provided with 512Mb of virtual address space, of which 32Mb is reserved for user program space. System software functions are embedded in the virtual address space of each process to make all functions immediately available on demand. This design reduces system overhead and promotes execution speed and efficiency.

Interleaved Main Memory

Main memory on the Prime 850 is expandable from 2Mb to 8Mb. All memory logic is Error Correcting and Checking (ECC) for dependable system integrity. Main memory uses efficient MOS storage devices with ultra-high storage density of 64 kilobit per chip on 1Mb boards.

Consecutive memory locations are on separate memory boards, so that two-way interleaving can be used to speed-up sequential memory accesses and maximize the cache hit rate. In effect, interleaving provides high-speed transfers between memory and the central processor by allowing the processor to read or write four or eight-bytes at a time. During burst mode, I/O, interleaving provides 64-bit data transfers for optimum performance of high-speed disk and magnetic tape subsystems.

The Prime 850 also supports 16-bit transfers for I/O devices and controllers, as well as half-word instructions such as 16-bit READS and WRITES. This preserves peripheral equipment investments and maintains total program compatibility with other Prime systems.

Stack Architecture

Prime 850 programs operate in a multi-segment environment that includes a stack segment containing all local variables, a pure instruction or procedure segment, and a linkage segment containing statically allocated variables and linkages to common data. Highly efficient addressing modes provide access to stack and linkage variables. Firmware implemented CALL and RETURN instructions eliminate the overhead of software stack management routines and argument passing.

The Prime 850 stack architecture optimizes the efficiency of operations such as parameter passing, subroutine and procedure calls, arithmetic expression evaluation, and dynamic allocation of temporary storage.

Instruction Set

The standard instruction repertoire is a compatible superset of the machine instructions available with other Prime systems. Addressing compatibility lets user programs written for any multi-user Prime system run without modification on the Prime 850 or any other Prime 50 Series system.

Over 500 instructions provide enhanced operating system communication, data handling and cooperating of processes. Highly flexible address formation techniques let all instructions use any of four user-access base registers, up to seven index registers, and 32-bit indirect words in any combination. This permits all memory reference instructions to reference the entire virtual address space.

The Prime 850 instruction capabilities exploit its 32-bit internal architecture and its 32-bit instruction and data paths. Of its eight 32-bit general purpose registers, seven can be used as index registers. These registers can also be used in local storage for compiler optimization or as fixed-point and logical accumulators. There are two floating-point registers, each 64-bits long, and two field address and length registers used by character and decimal instruction, also 64-bits long. Four other 32-bit registers include a procedure base, stack base, link base and auxiliary base register.

Integer Arithmetic Unit

The processor's 32-bit arithmetic unit performs all integer arithmetic and logical operations, significantly improving the execution times of integer arithmetic instructions. The arithmetic unit's design also efficiently handles complex address formations, such as base-plus-displacement and indexing.

Execution Control Unit

The Execution Control Unit uses a comprehensive set of firmware instructions to implement processor control mechanisms. Micro-instructions reside in read-only memory (ROM) with efficient 52-bit word length that is expandable to 64-bits. The microprogram is unaffected by power failures and is designed to implement user program instructions with maximum speed and efficiency.

One component of the Execution Control Unit is the Process Exchange facility. This facility automatically transfers the attention of either Instruction Execution Unit from one user process to another in order to maximize system throughput. Context switching mechanisms are implemented in both hardware and firmware for rapid process exchange and minimal system overhead.

System Integrity

The Prime 850 maintains system integrity through comprehensive error detection and reporting mechanisms. Microverification routines, invoked automatically when the system in initialized, test the validity of CPU logic and indicate any malfunction cause via a diagnostic status word. While the system is running, parity checking ensures data integrity throughout the processor's internal buses, registers, and other data paths. In addition, the Prime 850 automatically checks the parity of each microcode control word. Error-correcting codes in real memory automatically detect and correct all single-bit errors. (All two-bit errors are reported as well.)

A comprehensive, hardware-controlled memory protection system has a multi-ring protection hierarchy that allows programs to be assigned to any of several security levels. This gives multiple users full access to specified programs, protects other programs and databases from unauthorized access, and guards operating system software against accidental user intrusion.

Remote Diagnostics

The Prime 850 includes a sophisticated Virtual Control Panel (VCP) for local and remote system diagnostics capabilities. The VCP enables Prime support specialists to diagnose system problems that may originate in either hardware or software.

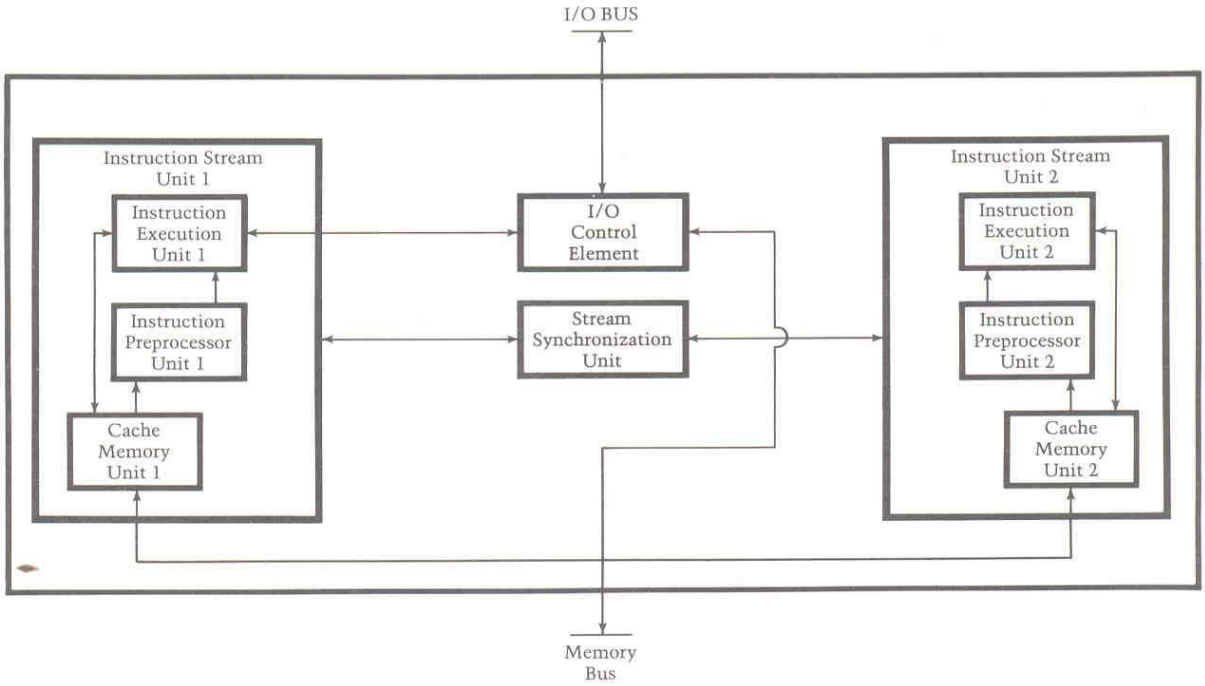
The local system operator or administrator initiates remote access simply by depressing a "Remote Enable" button on the VCP. A second button places the remote terminal in control mode, or gives the remote terminal the capability to control the system as if it were the local system console. The remote system administrator, when in control mode, can completely run the system from a remote terminal, including tasks such as bootloading and on-line operations.

Two VCP indicator lamps display the state of the remote communications link. One lamp indicates that a remote user has been authorized to monitor system operations. The second lamp indicates whether a remote access is in progress. A flashing lamp indicates that the remote user has been given the same control as the local system operator or administrator.

Software

The PRIMOS operating system supports both interactive and batch processes on all 50 Series systems.

The operating system supports reentrant procedures, permitting many different users to share a single copy of a software module, such as the text editor or FORTRAN compiler. PRIMOS further supports FORTRAN (ANSI '77), COBOL (ANSI '74), Pascal, PL/I (ANSI '76 Full and ANSI '80 Subset), BASIC/VM, RPG II, Prime Macro Assembler, the Source-Level Debugger, and the query and reporting facilities provided by PRIME/POWER. PRIMOS also supports DBMS, Prime's



CODASYL-compliant Database Management System; and the DBMS Query/Report Writer; MIDAS, the Multiple Index Direct Access System; FORMS, the Forms Management System; Prime/TAPS, the Terminal Application Processing System and Prime's Office Automation System. A wide variety of application packages are available from the Prime Users Library Service (PULSE) and from third-party software houses.

Input/Output

The Prime 850 supports a broad line of peripheral products for mass storage, interactive data entry/retrieval, and hard-copy output. System upgrades never require peripherals to be changed, because any peripheral can be used on any system.

Up to 2.4 billion-bytes of data can be stored on-line using Storage Module Disk subsystems. Magnetic tape products include a state-of-the art 75 ips 6250 bpi GCR unit, with up to eight tape drives available per system. Up to 128 different terminals can be used for local and remote input, for administrative functions of the Office Automation System, and as a system console. Finally, the range of printer options available includes a wide range of line printers (up to a high speed, 1000 line per minute printer), matrix line printer/plotter and a letter quality printer.

Networking

The Prime 850 supports networking and distributed processing with many different software and hardware communications products. PRIMENET™ networking software lets Prime computers communicate among themselves, with terminals, and with other manufacturers' systems by using a variety of communication facilities. These facilities allow users to log into other systems remotely, share files among systems, and develop distributed applications. Users can interface Prime computers to a range of terminals from communications lines with multiple protocols and remote job entry options: IBM BISYNC for HASP and 2780/3780; High-level Data Link Control (HDLC) protocol for X.25 packet switching networks; Control Data 200UT: Univac 1004; Honeywell GRTS: and ICL 7020.

Prime's Distributed Processing Terminal Executive (DPTX) allows the Prime 850 to emulate and support IBM 3271/3277 Display Systems.

The Prime 850 supports all of Prime's communications hardware controllers. User terminal communications are handled by the Asynchronous Multi-line Controller (AMLC). Communications for all of the synchronous software products are handled by the Multi-line Data Link Controller (MDLC), a controller handling multiple line protocols. For local area networks, the Prime 850 can be attached in a high speed ring network with any other 50 Series system. The ring network provides inter-system communication via a coaxial cable for up to fifteen Prime systems using PRIMENET networking software, with a data transmission band-width of eight megabytes.

Summary of Features	250-II	550-II	750	850
32-bit architecture	■	■	■	■
Simultaneous active processes	128	128	128	128
Direct connect terminal users	32	64	96	128
512Mb virtual address space per user	■	■	■	■
Bipolar cache memory	2KB	8KB	16KB	32KB
Instruction preprocessor unit			■	■
I/O bandwidth (Mb/SEC)	2.5	2.5	8	8
Multi-stream architecture				■
Hardware instructions for floating point arithmetic, decimal arithmetic and character string manipulations		■	■	■
Single and double precision floating point arithmetic	■	■	■	■
32-bit integer arithmetic	■	■	■	■
Microprocessor control unit with process exchange facility	■	■	■	■
Internal process or parity checking	■	■	■	■
Hardware Protection	■	■	■	■

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