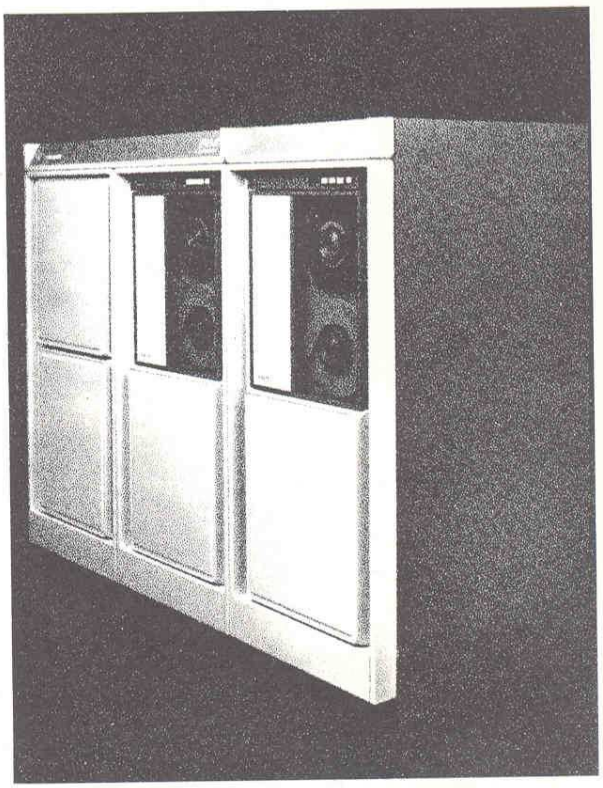
Product Bulletin

PRIME

Prime 750 System

Features

- Central system includes Prime 750 central processor with 32-bit architecture, 1M, 1.5M, 2M, 3M, or 4M bytes of error correcting MOS memory, 16-line asynchronous terminal controller, virtual control panel, system console, 14 board positions for peripheral or memory options, system cabinet and the PRIMOS® operating system.
- Up to 8 million bytes of error correcting MOS main memory.
- 32 million-byte virtual address space for each of up to 63 users.
- 16K-byte, 80 nanosecond cache memory.
- 64-bit interleaved memory data transfers.
- Instruction prefetch and decoding unit.
- Business instructions for decimal arithmetic, character manipulation and editing operations.
- Includes 32-bit integer arithmetic unit and hardware floating-point unit.
- High bandwidth (8 million-byte) burst mode I/O.
- Automatic microverification and parity checking throughout the system.
- Standard Virtual Control Panel for remote hardware and software diagnostics.
- Uses the PRIMOS operating system, for interactive, batch and multitask operations.
- Supports industry-standard languages including FORTRAN '77, ANSI '74 COBOL, Pascal, BASIC/VM, RPG II and PL/1, Prime's Office Automation System, and a wide variety of application software packages.



Description

The Prime 750 is the most powerful member of the 50 Series family of hardware- and software-compatible systems. It offers speed, low overhead, and flexibility in a wide range of computational timesharing and interactive data processing applications.

Central to the Prime 750's speed are a high-capacity cache memory, instruction prefetch unit, burst mode I/O, interleaved main memory and a high-performance floating-point unit. The Prime 750's efficient microcode structure ensures high-speed instruction execution. The number of microcode steps, as well as the time required for each step in an instruction execution cycle, are significantly lower than other systems. The Prime 750, for example, completes a 32-bit register-to-memory add instruction in only one machine cycle (micro-step).

The Prime 750 uses the multiterminal PRIMOS operating system. With PRIMOS, the Prime 750 can perform timesharing, batch and multitasking operations for up to 63 users. Each user has a 32 million-byte virtual address space and can use a variety of languages that simplify programming.

Performance Features

Business Instructions

The Prime 750 provides high-level support for ANSI '74 COBOL and other business-oriented languages with comprehensive instructions designed for decimal arithmetic, character field manipulation and editing operations.

COBOL decimal arithmetic operations support up to 18-digit packed or unpacked signed numbers. Operands—differing in data type and/or scale factor—are handled automatically during add, subtract, multiply, divide and comparison operations. Business instructions also allow rounding on numeric operations, and binary-to-decimal and decimal-to-binary conversions.

Character manipulation is peformed on field sizes of virtually any length. Justification, truncation, and padding are automatic in move, compare, translate, edit and similar operations. Numeric and character editing instructions let the user easily produce fields in ANSI '74 COBOL picture-like formats. For maximum efficiency, all business operations involve a limited number of on-line instructions.

Instruction Prefetch Unit

The instruction prefetch unit improves central processor performance by prefetching and decoding up to four instructions ahead of the program counter from cache memory. It accesses cache independently, so the next four instructions are prefetched, decoded and the effective address formed in parallel with instruction execution. When the processor's execution unit is ready for the next sequential instruction, it has been prepared in advance. This results in the Prime 750 spending more time executing and less time in fetching and decoding overhead.

Central logic in the instruction prefetch unit continuously fetches data from cache to keep the four instruction buffers full. In addition, the instruction prefetch unit can resolve most indirect addresses, further increasing instruction execution speed.

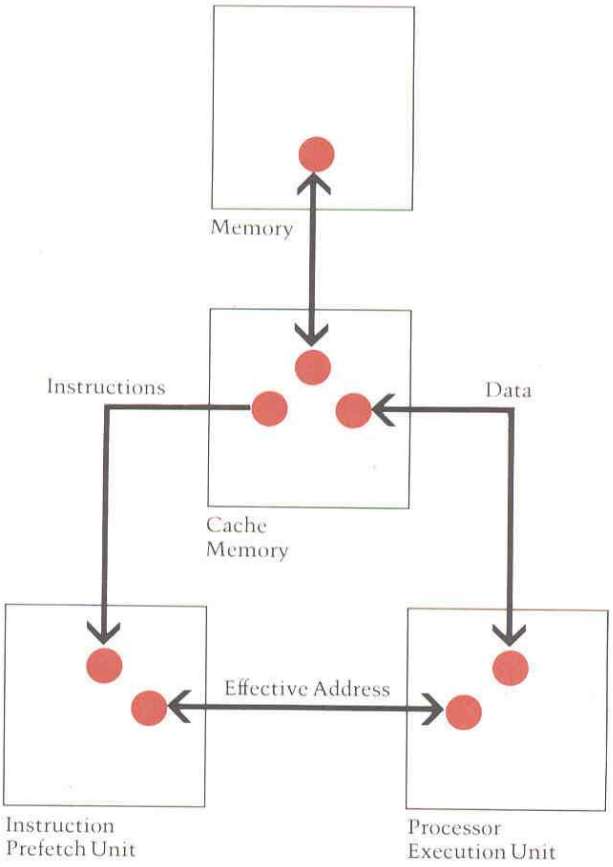


Figure 1: The instruction prefetch unit accesses cache memory independently of the central processor to perform instruction prefetch and decoding in parallel with execution.

Floating-Point Arithmetic

The Prime 750's 32-bit internal architecture uses microcode routines to implement single- or double-precision floating point instructions. With a 32-bit path between the unit and central processor, the floating-point unit accepts data at an extremely fast rate. Registers assigned to floating-point operations are integral to the unit itself, and its use of parallel logic permits exponential and fractional calculations to be done simultaneously. Separate parallel logic performs binary multiplication four bits at a time, division three bits at a time, and addition 48 bits at a time.

Cache Memory

A high-speed (80 nanosecond access) 16K-byte bipolar memory decreases the effective main memory cycle time to near that of the processor by storing data and instructions most likely to be used next by the processor. The cache, which is located on the central processor, eliminates memory bus delays in cache-to-processor transfers. Its high capacity provides a 95 per cent "hit rate" on anticipated processor requirements.

Both the instruction prefetch unit and the central processor's execution unit access cache memory. Memory mapping is completely overlapped with cache memory to further reduce total instruction execution times.

Integer Arithmetic Unit

The processor's 32-bit arithmetic unit performs all integer arithmetic and logical operations, significantly improving the execution times of integer arithmetic instructions. The arithmetic unit's design also efficiently handles complex address formations, such as base-plus-displacement and indexing.

Virtual Memory Management

The Prime 750 has virtual memory management facilities that provide multiple users with individual address spaces far in excess of the system's physical memory. Each system user gets a private and a shared system address space, which is divided into segments through automatic segmentation and paging. There are 256 segments (32 million bytes) available for each user, and the rest for shared operating system software. Operating system functions are embedded in each user's virtual memory space. This reduces system overhead by making all operating system functions immediately available, as if they were an integral part of a user's program.

Stack Architecture

Prime 750 programs operate in a multi-segment environment that includes a stack segment containing all local variables, an instruction or procedure segment, and a linkage segment containing statically allocated variables and linkages to common data. Highly efficient addressing modes provide access to stack and linkage variables. Hardware-implemented CALL and RETURN instructions eliminate the overhead of software stack management routines.

The Prime 750's stack architecture optimizes the efficiency of operations such as parameter passing, subroutine and procedure calls, arithmetic expression evaluation, and dynamic allocation of temporary storage.

Process Exchange

A process exchange facility automatically transfers the central processor's attention from one user (process) to another, with minimum overhead and complete protection. It allocates resources to the highest priority in a queue, and handles the logistics of processes ready for execution or waiting for a specific event to occur. The facility's firmware automatically dispatches a process for execution and reorders remaining processes without software intervention.

Interleaved Main Memory

Like all Prime systems, the Prime 750 uses MOS main memory and can address up to 8 million bytes of error checking and correcting (ECC) main memory.

Consecutive memory locations are on separate memory boards, so that two-way interleaving can be used to speed-up sequential memory accesses and maximize the cache hit rate. In effect, interleaving provides high-speed transfers between memory and the central processor by allowing the processor to read or write four or eight bytes at a time. During burst mode I/O, interleaving provides 64-bit data transfers for optimum performance of high-speed disk and magnetic tape subsystems.

The Prime 750 also supports 16-bit transfers for I/O devices and controllers, as well as half-word instructions such as 16-bit READS and WRITES. This preserves peripheral equipment investments and maintains total program compatibility with other Prime systems.

Register Sets

The Prime 750 has 128 32-bit hardware registers that are divided into four sections. One 32-bit register section handles firmware and operating system functions. Another controls the processor's 32 high-speed Direct Memory Access (DMA) channels. The remaining two sections hold the machine states of active processes. The process exchange facility dynamically and automatically manages register assignment to process.

Input/Output

The Prime 750 uses burst mode I/O that increases throughput and reduces central processor overhead. It provides an 8 million-byte-per-second transfer rate over the interface between the processor and peripheral controllers. This high bandwidth channel reduces the central processor's I/O load, and enhances the performance of high-speed peripherals.

The Prime 750 supports direct-to-memory I/O operations with Direct Memory Access (DMA), Direct Memory Control (DMC), Direct Memory Transfer (DMT), and Direct Memory Queue (DMQ) access modes.

The Prime 750 has 32 DMA channels controlled by high-speed channel address registers, which support an 8 million-byte-per-second transfer rate using burst mode I/O. High-speed peripherals such as disk subsystems typically use these channels.

DMC channels, controlled by channel address words in the first 8K-bytes of virtual memory, offer up to 2048 channels for medium-speed I/O transfers, like serial data communications. Their maximum transfer rate is 960K bytes-per-second.

DMT handles channel programs for high-speed device controllers, such as moving-head disk controllers. Maximum throughput rate is 2.5 million bytes-per-second.

DMQ channels provide circular queues for communication devices. The queues eliminate interrupt handling on a character-by-character basis, reducing system overhead.

Instruction Set

The standard instruction repertoire is a compatible superset of the machine instructions available with other Prime systems. Addressing compatibility lets user programs written for any multi-user Prime system run without modification on the Prime 750 or any other Prime 50 Series system.

Over 500 instructions provide enhanced operating system communication data handling and cooperating of processes. Highly flexible address formation techniques let all instructions use any of four user-access base registers, up to seven index registers, and 32-bit indirect words in any combination. This permits all memory reference instructions to reference the entire virtual address space.

The Prime 750 instruction capabilities exploit the 32-bit memory and cache data paths, and 32-bit internal architecture. Of its eight 32-bit general purpose registers, seven can be used as index registers. These registers can also be used in local storage for compiler optimization or as fixed-point and logical accumulators. There are two floating-point registers, each 64 bits long, and two field address and length registers used by character and decimal instructions, also 64 bits long. Four other 32-bit registers include a procedure base, stack base, link base and auxiliary base register.

System Integrity

The Prime 750 provides system integrity through comprehensive error detection and reporting mechanisms. Microverification routines, invoked automatically when the system is initialized, test the validity of the CPU logic and indicate any malfunction cause via a diagnostic status word. While the system is running, parity checking ensures data integrity throughout the processor's internal busses, registers, and other data paths. In addition, the Prime 750 automatically checks the parity of each microcode control word. Error-correcting codes in real memory automatically detect and correct all single-bit errors, so they are totally transparent to users. All two-bit errors are reported as well.

A comprehensive, hardware-controlled memory protection system has a multi-ring protection hierarchy that allows programs to be assigned to any of several security levels. This lets multiple users have full access to specified programs, protects other programs and databases from unauthorized access, and guards operating system software against accidental user intrusion.

Remote Diagnostics

The Prime 750 includes a sophisticated Virtual Control Panel (VCP) that allows a diagnostic specialist to locally or remotely control any system. This provides fast, effective troubleshooting, whether identifying a hardware problem or installing a new operating system revision.

The local system operator or administrator initiates remote access by simply depressing a "Remote Enable" button on the VCP. A second button places the remote terminal in control mode, or gives the remote terminal the capability to control the system as if it were the local system console. The remote system administrator, when in control mode, can completely run the system from a remote terminal, including tasks such as bootloading and on-line operations.

Two VCP indicator lamps display the state of the remote communications link. One lamp indicates a remote user has been given the ability to dial into the system and monitor operations. The second lamp indicates whether or not a remote access is in progress. If it is flashing, the remote user has been given the same control as the local system operator or administrator.

Software

The multiterminal PRIMOS operating system lets all Prime 50 Series systems perform interactive, batch and multitask operations. It supports reentrant procedures, permitting a single copy of a software module, such as the text editor or FORTRAN compiler, to be shared by many users. PRIMOS further supports ANSI '74 COBOL, ANSI '77 FORTRAN, BASIC, BASIC/VM, RPG II, PL/1, SPSS®, Pascal, Prime Macro Assembler, the Source-Level Debugger, and the various levels of query facilities provided by PRIME/POWER. PRIMOS also supports DBMS, Prime's CODASYL-compatible Database Management System; MIDAS, the Multiple Index Data Access System; FORMS, the Forms Management System; and Prime's Office Automation System. A wide variety of application packages, from other users and third-party vendors, is available from the Prime Users Library Service (PULSE).

Networking

The Prime 750 supports networking and distributed processing with an array of software and hardware communications products. PRIMENET™ lets Prime computers communicate among themselves, with terminals, and with other manufacturers' systems by using a variety of communication facilities. Users can interface Prime computers to a range of terminals from communications lines with multiple protocols and remote job entry options: IBM BISYNC for HASP and 2780/3780; High-level Data Link Control (HDLC) protocol for X.25 packet switching networks; Control Data 200UT; Univac 1004; Honeywell GRTS; and ICL 7020. Prime's Distributed Processing Terminal Executive (DPTX) software conforms to protocols used by IBM 3271/3277 Display Systems. And Prime offers hardware controllers for both synchronous and asynchronous communications.

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