PRIME Product Bulletin

PRIME 400

DESCRIPTION

The Prime 400 is a fast, large-capacity processor that offers an economical combination of high-speed computation and large virtual memory. Compatible with all other Prime processors, it runs software written for multi-user Prime 500, 350, and 300 systems and single-user Prime 100 and 200 systems. It runs programs up to 32 million bytes long. It supports up to 63 simultaneous users. It is logically compatible with all Prime peripherals, controllers, and I/O interfaces, so users can make plug-in upgrades from other Prime processors quickly and easily at a fraction of the total system cost. And its performance and capacity features give it up to a three-to-one speed increase over the Prime 300.

With features like cache memory, segmented and paged memory management and high-speed data transfer rates, the Prime 400 is a powerful and versatile processor for large-scale interactive data processing and computational timesharing systems. The Prime 400 is also ideally suited for distributed processing applications that off-load batch-oriented mainframes, and networks that use smaller Prime processors.

FEATURES

- Up to 32 million bytes of virtual address space per user
- Up to 63 simultaneous users
- Segmented and paged virtual memory management
- Optionally available error correcting MOS main memory expandable to 8 million bytes
- 2K-byte, 80 nanosecond access cache memory
- Embedded operating system for fast user access to all operating system resources
- Hardware-implemented rings of protection for system and user software security
- Automatic microprogrammed system integrity monitor
- Microcode word parity checking
- Hardware stack architecture to optimize shared procedures

PERFORMANCE FEATURES

Prime 400 users will be immediately aware of two fundamental characteristics: the processor is very fast, and the memory and peripheral configurations it supports are very large. The features of the processor's architecture responsible for the nearly three-to-one increase in speed compared to the Prime 300 are:

STACK ARCHITECTURE. Prime 400 programs operate in an environment consisting of a stack segment (containing all local variable values), an instruction or procedure segment, and a linkage segment

(containing statically allocated variables and linkages to common data). Especially efficient addressing modes are provided to access stack and linkage variables. Hardware implemented CALL and RETURN instructions eliminate software stack management routine overhead.

The Prime 400's stack structure optimizes the efficiency of such operations as parameter passing, subroutine and procedure calls, arithmetic expression evaluation and dynamic allocation of temporary storage and context switching.

CACHE MEMORY. A high-speed 80 nanosecond access 2K-byte, bipolar memory acts as a buffer between the central processor and main memory. Using a complex algorithm to determine what main memory information the central processor will most likely use, the cache memory significantly increases the apparent speed of the main memory. The cache algorithm assures a better than 85% "hit rate", reducing the effective main memory cycle time to approximately 400 nanoseconds. Memory mapping is completely overlapped with cache memory access, further reducing total instruction times.

HIGH-SPEED ARITHMETIC UNIT. The Prime 400 does all arithmetic and logical operations in its 32-bit-wide arithmetic unit. Processing data using a 32-bit format, rather than a 16-bit format, significantly improves the execution times of single- and double-precision integer and floating point arithmetic instructions. Also, the design of the arithmetic unit permits complex address formation, such as base plus displacement plus indexing calculations.

MICROPROGRAMMED CONTROL STORE. A comprehensive microcode structure reduces both the number of microcode steps and the time required for each step in an instruction execution cycle. For example, an add instruction is completed in two microcode steps, compared to five in the Prime 300.

INTERLEAVED MAIN MEMORY. The Prime 400 stores consecutive memory locations on separate memory boards, and uses two-way interleaving to speed up sequential memory accesses and maximize the cache hit rate. In effect, interleaving provides 32-bit transfers between the memory and CPU by allowing the processor to read or write two 16-bit words at a time.

DUAL REGISTER SETS. The Prime 400 processor has 128 32-bit hardware registers organized in two separate sets. These registers handle such functions as controlling the processor's 32 high-speed DMA channels and storing machine states during process exchange operations. The processor's process exchange mechanism dynamically and automatically assigns register sets to processes.

PROCESS EXCHANGE. A combination of hardware and firmware automatically allocates central processor resources to the highest priority process (a continuously executing sequence of machine code) in a queue of processes ready for execution. Process exchange handles the swapping of machine states necessary for coordinating between processes ready for execution and those waiting for a specific event to occur. Firmware within the process exchange mechanism automatically dispatches the next ready process of execution, without software intervention.

REAL & VIRTUAL MEMORIES

The Prime 400, like all other Prime central processors, uses MOS main memory. The processor can address up to 8 million bytes of main memory. Using 16K-bit memory chips, Prime offers up to 256K bytes of memory on a standard 16 x 18 inch (40.6 x 45.7cm) circuit board. The main memory's effective access time of 600 nanoseconds is nearly as fast as the central processor because of the Prime 400's 2K-byte cache memory. The cache is an integral part of the central processors, rather than being located on the main memory boards. This prevents memory bus delays from slowing down cache-to-processor transfers.

The Prime 400 uses virtual memory management facilities to provide multiple users with individual address spaces far in excess of the system's physical memory. These include both segmentation and paging, and provide all system users with individual virtual address spaces of 32 million bytes. Each user's address space consists of 128K-byte segments, half of which are available for user programs and half for PRIMOS operating system software. By embedding operating system functions in each user's virtual memory space, all operating system functions are immediately available as if they were an integral part of a user's program, reducing system overhead.

SYSTEM INTEGRITY FEATURES

The Prime 400 features powerful and flexible error detection capabilities. Parity checking is provided throughout the processor and main memory. Microverification routines, invoked either automatically or under program control, test the validity of the central processor's logic and use a diagnostic status word to indicate the cause of a malfunction. A machine-check mode of operation lets the user establish the remedial actions the system will take when it detects data errors or hardware fault conditions.

The processor is also equipped with a comprehensive, hardware-controlled memory protection system. A multi-ring protection hierarchy lets users assign programs to any of several security levels. Thus, multiple users can have open access to specified programs, while other programs and databases can be protected against unauthorized access, and operating system software can be guarded against accidental user intrusion.

INSTRUCTION SET

The Prime 400's instruction repertoire is a compatible superset of the machine instructions available with smaller Prime central processors. Addressing mode compatibility assures that user programs written for any other Prime processor can run on the Prime 400 without modification.

In addition to its compatibility with smaller Prime processors, the Prime 400 offers unique addressing modes and instructions that significantly expand its processing power. Over 80 instructions, including 32-bit arithmetic, NOTIFY and WAIT, and conditional store, provide better operating system communication, enhanced data handling capabilities and cooperating process communication. Also, enhanced address formation allows all instructions, both new and old, to use any combination of four user-accessible base address registers, two index registers and 32-bit indirect words. This permits all instructions to reference a virtual memory space of up to 32 million bytes, compared to the Prime 300's 128K-byte maximum.

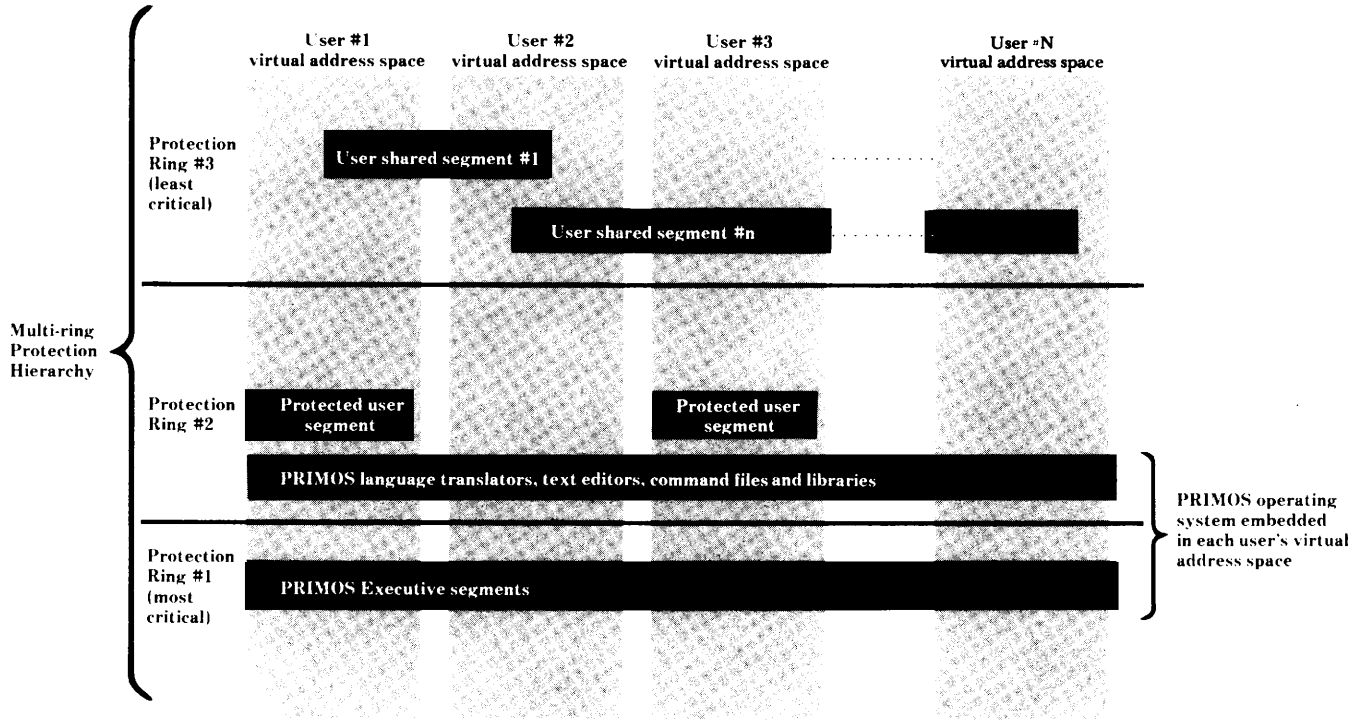
INPUT/OUTPUT

Direct-to-memory input/output operations are supported by three types of program-assignable I/O channels. Thirty-two program-assignable DMA channels, controlled by high-speed channel address registers, provide high throughput with a minimum of central processor control overhead. The channels have a maximum data rate of 2.5 million bytes per second. DMC channels, controlled by channel address words in the cache memory, offer an unlimited number of channels for medium-speed I/O transfers. The DMC channels have a maximum transfer rate of 960K bytes per second. DMT channels are provided for device controllers, such as the controllers for moving-head disks, that execute channel control programs. The maximum DMT throughput rate is 2.5 million bytes per second.

In addition to these direct-to-memory channels, a DMQ mode of operation provides a circular queue for handling communication devices. The queue reduces operating system overhead by eliminating interrupt handling on a character-by-character basis.

SYSTEM SOFTWARE

A single, multifunction operating system—PRIMOS—provides all control functions necessary to support multiterminal, batch, and multitask real-time operations. PRIMOS is embedded in each user's virtual memory space, assuring rapid access to operating system resources by user programs. The operating system supports shared, reentrant procedures, so multiple users can share a single copy of a software module, such as a FORTRAN compiler. In addition to FORTRAN IV, PRIMOS also supports BASIC, BASIC/VM, ANSI '74 COBOL, RPG II, and Macro Assembler languages. PRIMOS includes database-oriented file management resources that permit multiple keyed accesses to on-line data bases.



PRIMOS VIRTUAL MEMORY MANAGEMENT

PRIME 400 CPU

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PRIME

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