PRIME Product Bulletin

PRIME 500

DESCRIPTION

The Prime 500 is the newest and most powerful member of Prime's family of hardware- and software-compatible central processors. It runs software previously written for single-user Prime 100 and 200 systems, as well as user programs written for multiuser Prime 300 and 400 systems, without modification. And since it is logically compatible with all Prime peripheral devices, controllers and I/O interfaces, plug-in upgrades from other Prime processors are easily accommodated at a small fraction of the total system cost. The Prime 500 also offers new performance enhancements for floating-point arithmetic, decimal arithmetic, character manipulation and editing operations, and can provide better than a three-to-one performance improvement, depending on the instruction mix, over the Prime 400.

With features such as cache memory, segmented memory management and new high-speed instructions, the Prime 500 is a powerful and versatile base for large-scale Prime systems providing interactive data processing and computational timesharing services. The Prime 500 is also ideally suited for distributed processing applications involving the off-loading of batch-oriented mainframes and networks including smaller Prime processors.

FEATURES

- 32M-byte virtual address space
- Up to 63 simultaneous users
- Segmented and paged virtual memory management
- Error correcting MOS main memory expandable to 8M bytes
- 2K-byte, 80 nsec access cache memory
- Business instructions for decimal arithmetic, character manipulation, and editing operations
- High-speed floating-point arithmetic unit
- 32-bit arithmetic unit
- Dual sets of 64, 32-bit registers for fast context switching via process exchange
- Eight, 32-bit general registers
- 32-bit internal decor
- Embedded operating system for fast user access to all operating system resources
- Hardware-implemented rings of protection for system and user software security
- Automatic microprogrammed system integrity monitor
- Microcode word parity checking
- Hardware stack architecture to optimize shared procedures

PERFORMANCE FEATURES

Users of the Prime 500 will be immediately aware of two fundamental characteristics: the processor is very fast, and the memory and peripheral configurations it can support are very large. The processor shares many of the high-performance features of the Prime 400 and adds to this performance base a new, high-speed floating-point arithmetic unit, direct hardware execution of business instructions, and an expanded instruction set that supports the processor's eight general registers. The most significant features of the Prime 500's architecture responsible for its high performance levels are described below.

BUSINESS INSTRUCTIONS. The Prime 500 provides high-level support for ANSI '74 COBOL and other business-oriented languages through comprehensive instructions designed for decimal arithmetic, character field manipulation, and editing operations.

Decimal arithmetic operations support packed or unpacked signed numbers of up to 18 digits. Operands differing in data type and/or scale factor are automatically handled during add, subtract, multiply, and divide, and comparison operations. Rounding may be specified on numeric operations and instructions are provided for binary/decimal and decimal/binary conversions.

Character operations can be performed on field sizes of virtually any length. Operations for moves, compares, translates, searches, etc. automatically handle justification, truncation, and padding. Numeric and character editing instructions are provided which easily produce fields in ANSI '74 COBOL-like picture formats.

Business-type operations are performed with a limited number of in-line instructions and, depending on the instruction mix, performance can be improved three or more times compared with the Prime 400.

FAST FLOATING-POINT ARITHMETIC. Users of Prime 500 systems can expect instruction execution times for single- and double-precision floating-point arithmetic to be comparable to those of the considerably more expensive IBM System 370 Model 158. Users upgrading from a Prime 400 can run all existing programs without any modification, and can expect an approximate three-to-one improvement in floating-point instruction performance, depending on the particular floating-point instructions involved.

One of the reasons for the Prime 500's fast floating-point speeds is the use of parallel logic in the floating-point arithmetic unit. Thus, binary multiplication is done four bits at a time, division is done three bits at a time and addition 48 bits at a time. This is significantly faster than the single bit algorithms traditionally used for multiply and divide. Separate logic handles exponents, control, and interim values, so that exponent and fraction calculations are done concurrently with arithmetic processing.

TYPICAL FLOATING-POINT TIMES CHART

Instruction	Prime 400	Prime 500	IBM 370/158
Single Precision			
Add	5.18 μsec.	3.72 μsec.	2.4 μsec.
Multiply	9.00	4.02	2.3
Divide	11.92	6.40	8.9
Double Precision			
Add	6.46	4.80	2.2
Multiply	20.14	6.46	3.6
Divide	24.04	8.68	23.2

STACK ARCHITECTURE. Prime 500 programs operate in an environment consisting of a stack segment (containing all local variable values), an instruction or procedure segment, and a linkage segment (containing statically allocated variables and linkages to common data). Highly efficient addressing modes are provided to access stack and linkage variables. Hardware implemented CALL and RETURN instructions eliminate the overhead of software stack management routines.

The Prime 500's stack structure has been designed to optimize the efficiency of such operations as parameter passing, subroutine and procedure calls, arithmetic expression evaluation and dynamic allocation of temporary storage and context switching.

CACHE MEMORY. A high-speed (80 nanosecond access) 2-K byte, bipolar memory acts as a buffer between the central processor and main memory. Using a complex algorithm to determine the main memory information that will most likely be used next by the central processor, the cache memory increases the apparent speed of the main memory to near that of the processor. The cache algorithm assures a better than 85% "hit rate". Memory mapping is completely overlapped with cache memory access for further reduction of total instruction execution times.

HIGH-SPEED INTEGER ARITHMETIC UNIT. All integer arithmetic and logical operations are performed in the processor's 32-bit wide arithmetic unit. Using a 32-bit format, rather than a 16-bit format, significantly improves the execution times of single- and double-precision integer arithmetic. Additionally, the design of the arithmetic unit permits complex address formation, such as base plus displacement and indexing, to be efficiently handled.

MICROPROGRAMMED CONTROL STORE. A highly efficient microcode structure, like that used on the Prime 400, assures high-speed instruction execution. The number of microcode steps as well as the time required for each step in an instruction execution cycle has been significantly reduced compared to smaller Prime processors, so that an add instruction, for example, is completed in two microcode steps versus five on a Prime 300.

INTERLEAVED MAIN MEMORY. Consecutive memory locations are on separate memory boards so that two-way interleaving can be used to speed up sequential memory accesses and maximize the cache hit rate. In effect, interleaving provides 32-bit transfers between memory and CPU by allowing the processor to read or write two 16-bit words at a time.

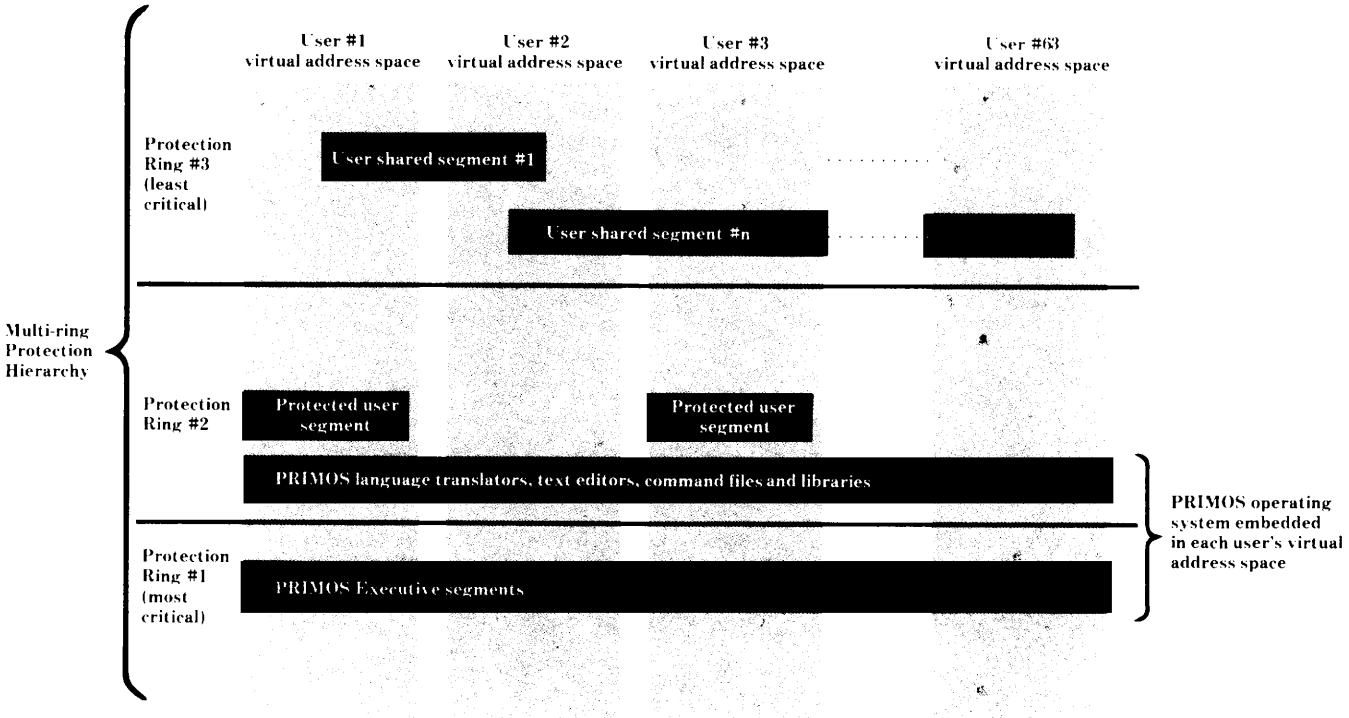
DUAL REGISTER SETS. The processor is equipped with 128, 32-bit hardware registers. These registers handle a variety of functions such as controlling the processor's 32 high-speed DMA channels and storing machine states in dual register sets during process exchange operations. Assignment of these register sets to processes is managed dynamically and automatically by the process exchange mechanism of the processor.

PROCESS EXCHANGE. A combination of hardware and firmware automatically controls the allocation of CPU resources to the highest priority process (a continuously executing sequence of machine code) in a queue of processes ready for execution. Process exchange handles the swapping of machine states necessary for coordinating between processes ready for execution and those waiting for a specific event to occur. Firmware within the process exchange mechanism automatically dispatches the next ready process for execution, without software intervention.

REAL & VIRTUAL MEMORIES

The Prime 500, like all other Prime CPU's, uses MOS main memory exclusively. The processor can address up to 8M bytes of main memory. The main memory's access time of 600 nanoseconds is reduced to near that of the central processor through the use of a 2K byte cache memory. The cache is an integral part of the CPU, rather than being located on the main memory boards, thereby preventing memory bus delays from slowing down cache-to-processor transfers.

To provide multiple users with individual address spaces far in excess of the physical memory available with a system, the Prime 500 CPU is equipped with virtual memory management facilities. These facilities include both segmentation and paging, and provide all system users with individual virtual address spaces. Each user's address space consists of 128K-byte segments, half of which are available for user programs and half for PRIMOS operating system software. By embedding operating system functions in each user's virtual memory space, all operating system functions are immediately available as if they were an integral part of a user's program, thereby reducing system overhead.



PRIMOS VIRTUAL MEMORY MANAGEMENT

PRIME 500 CPU

System Integrity Features

The Prime 500 shares the same powerful and flexible error detection features available on the Prime 400. Parity checking is provided throughout the processor and main memory. Microverification routines can be invoked, either automatically or under program control, to test the validity of the CPU's logic and indicate, via a diagnostic status word, the cause of a malfunction. A machine-check mode of operation allows the user to establish the remedial actions the system will take upon detection of data errors or hardware fault conditions. Additionally, the parity of each control word (microcode) is automatically checked.

The processor is also equipped with a comprehensive, hardware-controlled memory protection system. A multi-ring protection hierarchy allows programs to be assigned to any of several security levels. Thus, multiple users can have open access to specified programs, other programs and databases can be protected against unauthorized access, and operating system software can be guarded against accidental user intrusion.

Instruction Set

The Prime 500's instruction repertoire is a compatible superset of the machine instructions available with smaller Prime CPU's. Addressing mode compatibility is also provided so that user programs written for any single-user Prime 100 or 200 or any multiuser Prime 300 and 400 will run without modification on the Prime 500.

The Prime 500 features instructions that support the processor's eight general registers, and instructions for decimal arithmetic, character manipulation, and editing operations.

A set of approximately 80 instructions, including 32-bit arithmetic, NOTIFY and WAIT, and conditional store, provide enhanced operating system communication, data handling and cooperating process. Also, highly flexible address formation techniques in the Prime 400 and 500 allow all instructions to use any of four user-accessible base address registers, two index registers and 32-bit indirect words in any combination. This permits all instructions to reference a virtual memory space of 32M bytes, compared to a 128K-byte maximum for the Prime 300.

Input/Output

Direct-to-memory input/output operations are supported by three types of program-assignable I/O channels. Thirty-two, program-assignable DMA channels are controlled by high-speed channel address registers and provide high throughput with a minimum of CPU control overhead. The maximum data rate supported by these channels is 2.5 million bytes per second. DMC channels, controlled by channel address words in the first 8K bytes of main memory, offer an unlimited number of channels for medium-speed I/O transfers to a maximum transfer rate of 960K bytes per second. DMT channels are provided for device controllers, such as the controllers for moving-head disks, that execute channel control programs. The maximum DMT throughput rate is 2.5M bytes/second.

In addition to these direct-to-memory channels, a DMQ mode of operation provides a circular queue for handling communication devices. The queue reduces operating system overhead by eliminating interrupt handling on a character-by-character basis.

System Software

A single multi-function operating system—PRIMOS V—provides all control functions necessary to support multi-terminal, queued and multitask real-time operations. PRIMOS V is embedded in each user's virtual memory space to assure rapid access to operating system resources by user programs. The operating system supports shared, reentrant procedures, permitting a single copy of a software module such as a FORTRAN IV compiler to be shared by multiple users. PRIMOS V supports ANSI '74 COBOL, FORTRAN IV, BASIC, RPG II, and Macro Assembler Languages; both levels of Prime data management systems, DBMS, the CODASYL-compliant Database Management System and MIDAS, the Multiple Index Data Access System for multiple entry point access of keyed files; and FORMS, the Form Management System for manipulation of video and hardcopy terminals.

PRIME

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