Prime Computer Logic Diagrams

MAGNETIC TAPE CONTROLLER

MPC 2 E.V.

LOGIC DIAG. LDS 1811

Prime Computer, Incorporated, 145 Pennsylvania Avenue, Framingham, Massachusetts 01701

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DWG. NO.	DATE	REV.
LDS 1811		

Magnetic Tape Programming

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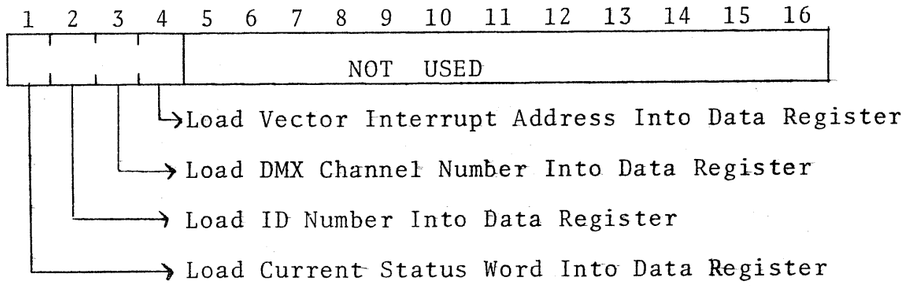
INA 00XX	Input Data Register
OTA 01XX	Motion Setup
OTA 02XX	Setup Data Register
OTA 03XX	Power On
OTA 14XX	DMA/C Channel #
OTA 16XX	Interrupt Vector Address

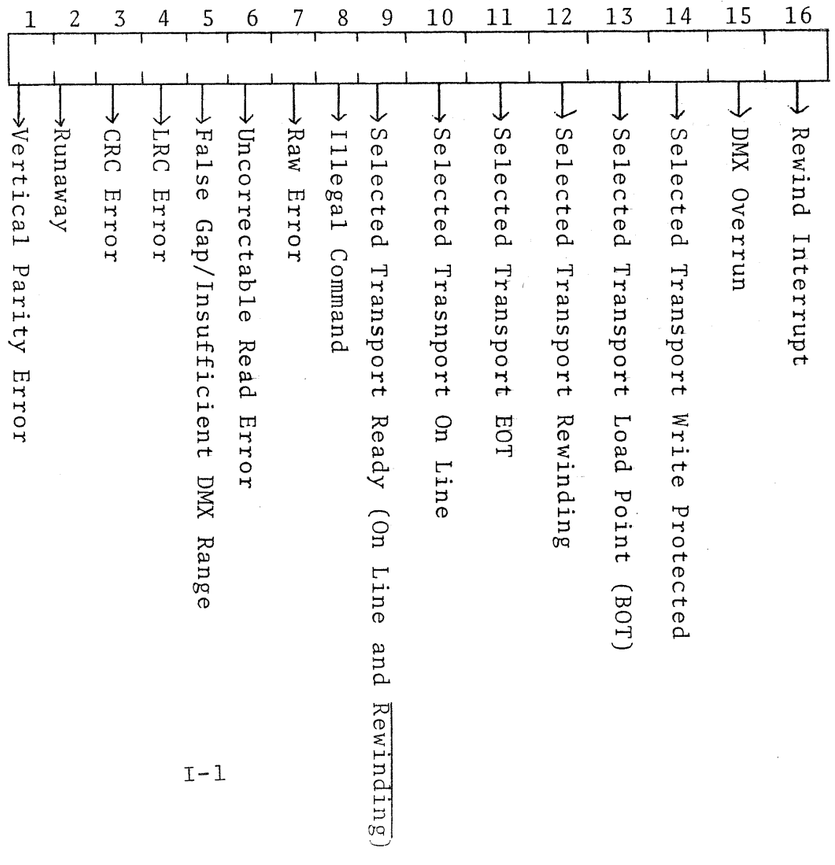
OTA 02XX Setup Data Register

This OTA sets up the Data Register which is Input via an INA 00XX.

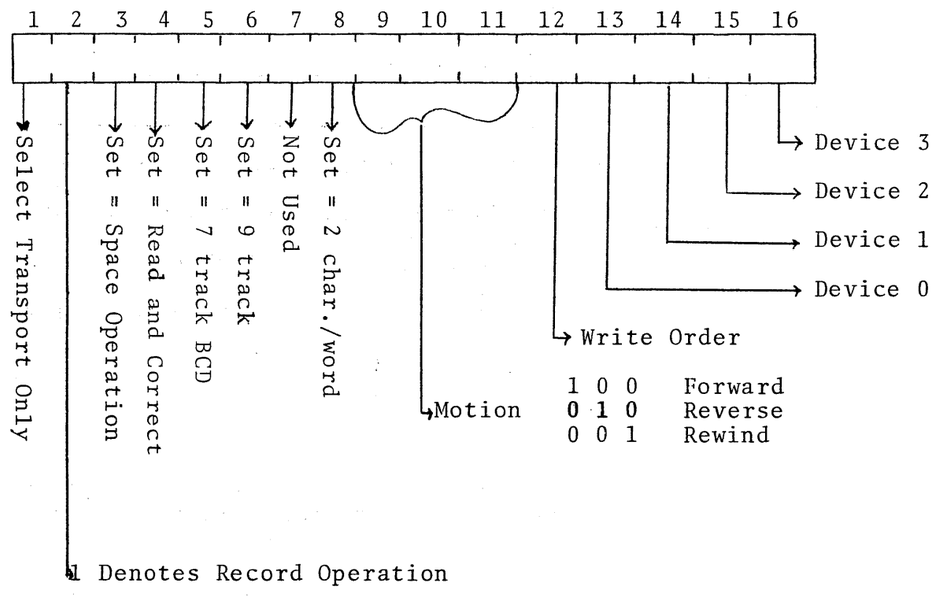


Status Word

The Controller maintains a status of the operation just completed and the transport last selected.



OTA 01XX Motion Setup



1 Denotes Record Operation

0 Denotes File Operation

Setup Word combinations for OTA 01XX

	HEX.	OCTAL
Write Record, one char/word	449X	04222X
Write Record, two char/word	459X	05262X
Read Record, one char/word	448X	04220X
Read Record, two char/word	458X	04260X
Read and Correct, one char/word	548X	05220X
Read and Correct, two char/word	558X	05260X
Write File Mark	249X	02222X
Forward One Record	648X	06220X
Forward One File	248X	02220X
Backspace One Record	644X	06210X
Backspace One File	244X	02210X
Rewind	002X	00004X
Select Transport	800X	10000X

MPC Register File Usage

RF0	Scratch
RF1	Scratch
RF2	Image of DR2
RF3	Status Word (LB)
RF4	Image of DR4/Status Word (RB)
RF5	Delay Count
RF6	Program Phase Bits (See below)*
RF7	Long Delay Count
RF8	Longer Delay Count
RF9	Char. Count Reg. 1 or 2 char./words
RF10	Left Data Byte
RF11	Right Data Byte
RF12	Bit 1, parity of RF11
RF13	Write Byte Count Register
RF14	Scratch used for CRC/EPR calculation
RF15	Cyclic redundancy check register (CRCR) $CRC_o \rightarrow 7$
RF16	Cyclic redundancy check register (CRCR) CRC_p (bit 1)
RF17	Error position register (EPR) $EPR_o \rightarrow 7$
RF18	Error position register (EPR) EPR_p (bit 1)
RF19	LRC register $LRC_o \rightarrow 7$
RF20	LRC register LRC_p in bit 7
RF21	Zero constant
RF22	9T/7T constant (Write), Frame count (Read)
RF23	Track error register ch p (bit 7)
RF24	DMX channel number (LB)
RF25	DMX channel number (RB)
RF26	Track error register channels 0-7
RF27	Interrupt vector address (RB)
RF28	Rewind status register
RF29	Setup word, left byte
RF30	Setup word, right byte (DR3 similar)
RF31	Interrupt vector address (LB)

*Note:

RF6	Bit 8	Odd/even count
	7	All data written
	6	Write CRCC
	5	Write LRCC
	4	Read CRCC
	3	
	2	
	1	

Device Register Usage

DR1 — Bits 1-8, WDo-7 Write Data

DR2 — Bit 1, Parity of DR1, Wp
Bit 7, WARS, LRCC STB
Bit 8, WDS, WRITE STB

DR3 — Bits 5-8, Select 0-3
Bit 1 SFC Forward
Bit 2 SRC Reverse
Bit 3 RWC Rewind
Bit 4 SWS Write

DR4 — Bit 1 RDY, Online & not rewinding
2 Online
3 EOT End of Tape
4 RWD Rewind
5 LDP, BOT
6 FPT, File Protect
7 LOL, Load & Online

DR5 — Bits 1-8 RDO-7 Read Data

DB8 — Bit 7 Read Parity RDP
3 RDS, Read STB

DB7 — Bit 8 DDI Density

LTR	DATE	REVISION	DR.	CK.
A	3-28-74	Sheet 5 per ECN 1298		

MATERIAL	DWN	PRIME COMPUTER INC. NATICK, MASS.		
	CHK			
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES –DIMENSIONS ARE IN INCHES –TOLERANCES xx ± .02 xxx ± .005 ANGLES ± 1/2°	ENG.	NRZ1 Magnetic Tape Controller Product Specification		
	APPRD			
USED ON	SCALE	SIZE	DWG. NO.	REV.
NEXT ASSY 4020-XXX	SHEET 1 OF 17	A	SPC0642	A

LTR	DATE	REVISION	DR.	CK.

1.0 GENERAL

The NRZ1 magnetic tape controller will control reading, writing and spacing operations on up to 4 magnetic tape transports.

2.0 APPLICABLE DOCUMENTS

Micro-programmed controller product specification (reference A)
I/O bus specification (reference B)

3.0 TAPE TRANSPORT FEATURES

3.1 The transports will fall into one of the following two families:

3.1.1 Seven track, compatible with IBM 729 standards, recording tape at 556 or 800 bits/inch.

3.1.2 Nine track, compatible with IBM 360/ANSI standards for 800 bits/inch NRZ1 recording.

3.2 Further details of the tape transports used are as follows:

- o Tape speed of 45 inches per second.
- o Reel size is up to 10.5 inches diameter; reels to be IBM compatible.
- o Rewind speed to be 150 inches per second minimum.
- o Start/Stop distances to be 0.19 inches.
- o Transports are rack mountable (19" EIA), approximately 24 inches high and weigh not more than 90 pounds.
- o Operating temperature and humidity to be 4°C to 32°C and 20 to 80%, respectively.
- o Have a "daisy chain" capability such that up to four transports may be installed in a system.
- o Each transport to be equipped with a unit select switch so that any drive can assume any logical address.
- o Electrical and mechanical interface to be "industry standard." This means compatible with Pertec 8000 Series transports.
- o Transport power to be 47-400 Hz, 95-250 volts (single phase) by changing AC connections only.

4.0 CONTROLLER CAPABILITY

4.1 The following functions are provided in the controller:

	USED ON	SCALE	SIZE	DWG. NO.	REV.
	NEXT ASSY	SHEET 2 OF 17	A	SPC0642	A

Write binary record at one character per word.
Write binary record at two characters per word.
Write BCD record (7 track only) at one character per word.
Write BCD record (7 track only) at two characters per word.

Read binary record at one character per word.
Read binary record at two characters per word.
Read BCD record (7 track only) at one character per word.
Read BCD record (7 track only) at two characters per word.

Read binary record (9 track only) at one character per word and correct errors.
Read binary record (9 track only) at two characters per word and correct errors.

Write file mark.
Space forward one record.
Space forward one file.
Backspace one record.
Backspace one file.
Rewind.
Select transport.

4.2 Character packing

The one or two characters per word referred to in paragraph 4.1 is defined further in this section.

Figure 1 shows the 16 bit computer word/tape channel relationship for one character per word mode. For 9 track recording, bits 9-16 are written on tape; for 7 track recording, bits 11-16 are written on tape. When reading tape in this mode, the left byte will be transferred to the computer as zeros as will bits 9 and 10 when reading from a seven track transport.

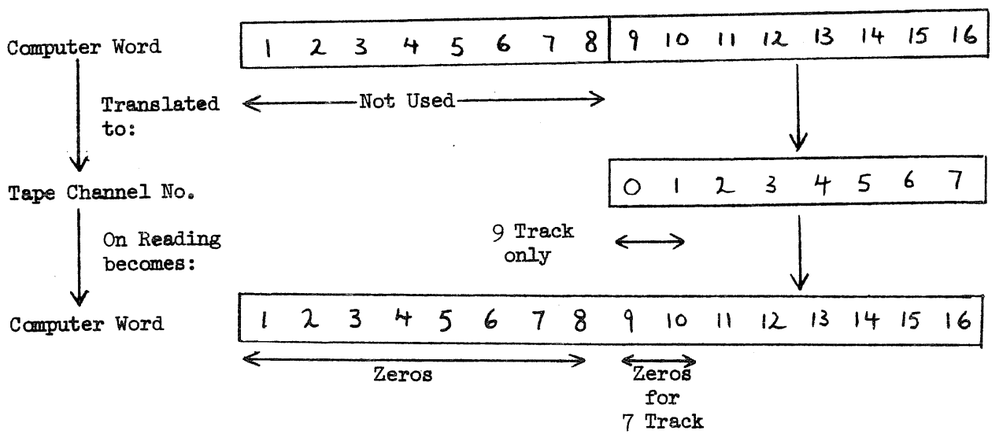


FIGURE 1

Figure 2 shows how two characters per word byte packing is organized. When reading data from a seven track transport, bits 1, 2, 9 and 10 will be transferred to the computer as zeros.

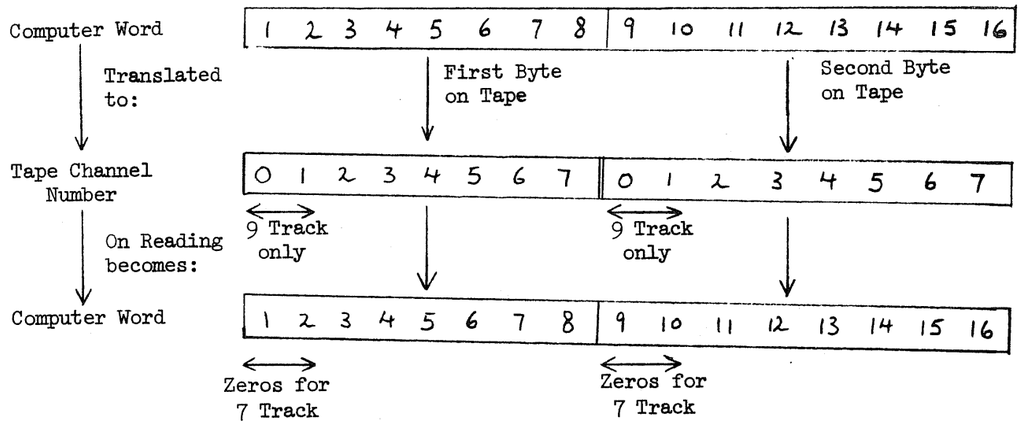
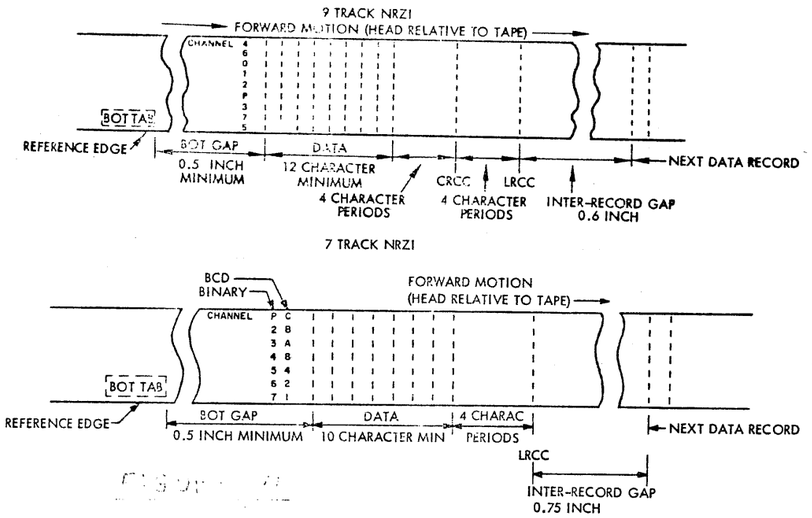


FIGURE 2

4.3 Format on tape

The tape formats for seven and nine track recording are shown in figure 4. Principal differences between the two are as follows:



- As both formats use the same width tape, track width and inter-track spacing are narrower for nine track compared to seven track.
- Nine track format has a cyclic redundancy check character (CRCC) inserted between the end of the record and the longitudinal redundancy check character (LRCC). The CRCC, in addition to providing a greater degree of data integrity, gives the capability of error correction in the case of a "hard error." This is explained in more detail in paragraph 4.9 below.
- Inter-record gap is 0.15" shorter for 9 track operation and this gives more data storage per reel of tape.
- Track numbering is different between the two formats but in each case agrees with the track numbers given in figures 1&2. The nine track numbering scheme is designed to give an incremental reliability advantage by placing the most important tracks in the center of the tape.
- The minimum data record sizes shown in figure 4 are IBM standards. The PRIME system is capable of writing (and reading) records as short as three characters.

4.4 Binary/BCD records

Reference is made in paragraph 4.1 to writing and reading binary and/or BCD records. This applies to 7 track transports only. A binary record will have odd vertical parity (channel P on tape). A BCD record will have even vertical parity on tape. The code $(00)_8$ from/to computer memory is translated to $(12)_8$ when written onto/read from tape. This translation is performed by the controller and eliminates the problem of an all zeros character on tape appearing as a missing frame.

4.5 File mark (tape mark)

One or more records on tape form a file. Files are designated by two special characters recorded on tape and these are shown in figure 5.

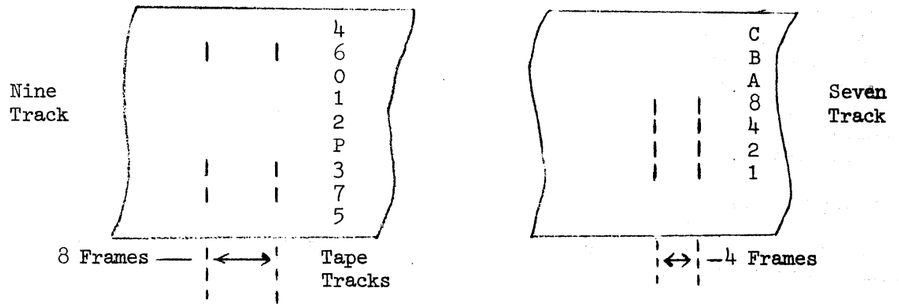


FIGURE 5

In both cases the file mark is separated from the previous record by 3.5 inches of blank tape and by the normal inter-record gap from the next record (0.6 or 0.75 inches). "Previous" is with reference to the tape running in the forward direction as the file mark is recorded with the tape moving forward only.

4.6 Spacing operations

The tape transport can be commanded to space forward or backwards either a record or a file. No data is transferred to the central processor for any of these operations although the controller will read data from the tape to determine when to stop tape motion. In the case of a "backspace file" operation, tape motion will stop with the transport read/write head in the 3.5 inch gap between the last record written and the file mark.

4.7 Writing and reading operations

These are done in the forward direction only. The controller is not capable of writing or reading data records in reverse.

4.8 Tape updating

It is not possible to selectively update records written on the tape. This applies even if the new record is the same length as the old one. After starting to rewrite a tape from a certain record, all further records down the tape should

be considered as invalid and unreadable. The reason for this restriction (typical for all IBM compatible tape systems) is concerned with inter-gap noise transients and worst case tolerances.

4.9 Read and correct operations

As mentioned previously, a CRCC is recorded on tape at the end of each record written on a nine track transport. The CRCC provides a more powerful error detection scheme than that provided with the seven track format (vertical parity and LRCC only).

When a record is read, the CRCC is recomputed on a frame by frame basis and effectively compared with the CRCC recorded on the tape. If they disagree, the record has been read incorrectly and the controller is able to determine which track is in error provided the error(s) have occurred in a single track. (As the track to track spacing is 44 times greater than the bit to bit spacing, errors in multiple tracks are unusual.) To correct the error, the record must be re-read in the forward direction. As each character is read from tape, its vertical parity is checked (as usual) and if found to be in error, a correction is made to the data in the track determined before to be in error during the previous read operation. Should the read error switch tracks during the second read operation, the CRC calculation won't balance and a second re-read will be required.

Before the controller is instructed to "read and correct" a record, standard error recovery techniques should be tried. An example of this is as follows:

- o Read forward one record. Backspace a record if an error is detected and re-read forward up to a total of 6 times.
- o If unsuccessful, backspace four records (or to load point if less than four records away), space forward three records and then read the problem record. This sequence draws the tape over the tape cleaner and could dislodge a possible dirt particle. Try this sequence a total of 6 times.
- o If unsuccessful, attempt "read and correct" if the controller has determined that the error can be corrected. As detailed in section 7.1 below, there are situations, other than a multi-track error, which can cause the record to be uncorrectable.

5.0 PROGRAMMING DETAILS

5.1 Transport configuration

Up to four transports may be attached to the controller. They may be 7 track, 9 track or a mixture of both. The controller is unaware of the difference and it is the responsibility of the magnetic tape driver routines to issue meaningful instructions to the appropriate transports (e.g., a "read and correct" operation to a 7 track transport is illegal).

The four transports are assigned logical addresses from 0-3 (see paragraph 5.6 below). Each transport has a selection dial which may be set from 0-3 to respond to any of the four addresses. If more than one transport is dialed to the same address, results will be undefined.but no physical damage will occur.

When a reel of tape is loaded on a 7 track transport, the appropriate density of recording must be manually selected.

5.2 PIO commands

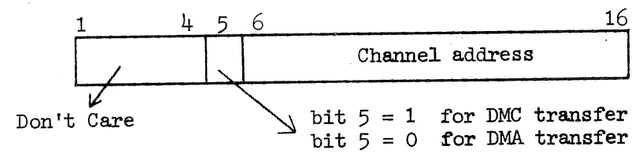
Table 1 shows the PIO commands that are implemented in the controller. Data transfers between the controller and memory are by using DMA/C only. The function of the OCP commands is explained in reference A. Other commands are explained below.

5.3 Controller address

The controller responds to address $(14)_8$.

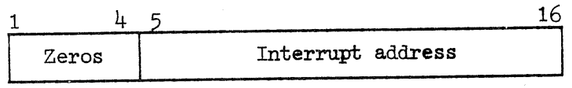
5.4 OTA 14, DMA/C channel number

The format for this instruction is standard and is as follows:



5.5 OTA 16, Interrupt vector address

The format for this instruction is as follows:



If an interrupt vector address is not specified, the controller will assume an address of $(114)_8$ and will interrupt via this location. Following an OTA 16, the controller will maintain the specified interrupt address until initialized when the address will revert to $(114)_8$.

5.6 OTA 01, Motion setup

This OTA is used to select one of four transports and to initiate some action from that transport. For reading and writing orders, the DMA/C Channel address OTA should be given prior to this OTA. A register bits of the motion setup OTA are defined as follows:

Bit 1 "1" denotes Select transport only. All other bits of the setup word are ignored except 9-12.

Bit 2 "1" denotes a record operation.
"0" denotes a file operation.
For example, this bit is set for Backspace a record but cleared for Write file mark.

Bit 3 "1" denotes a [illegible] spacing operation such as Forward a Record. Bit 3 should be cleared for reading and writing record operations.

Table 1

PIO Commands

Function Code Bits 7-10 \ Op Code Bits 1-6	14₈ (OCP)	34₈ (SKS) (SKIP IF)	54₈ (INA)	74₈ (OTA)
00		Ready	Input data register	
01		Not Busy		Motion Setup
02				Housekeeping Setup
03				Load and On-Line
04		Not Interrupting		
05				
06				
07		Status Incorrect		
10				
11				
12	Set Normal Mode			
13	Set Diagnostic Mode			
14	Acknowledge Interrupt			DMA/C Channel#
15	Set Int Mask			
16	Clear Int Mask			Int Vector Add
17	Initialize			

Bit 4 "1" denotes that a read operation is to be a 9 track transport "Read and Correct."

Bit 5 This bit applies to 7 track transport operation only and should be set for BCD write and read orders and cleared for binary write and read orders.

Bit 6 This bit should be set when an order is directed to a 9 track transport. Rewind and select orders don't care about this bit.

Bit 7 Not used.

Bit 8 Set for two character/word data transfers.

Bit 9 Set for forward motion on the selected transport. Bits 10, 11 to be cleared.

Bit 10 Set for reverse motion on the selected transport. Bits 9, 11, 12 to be cleared.

Bit 11 Set for a rewind (to load point) or the selected transport. Bits 9, 10, 12 to be cleared.

Bit 12 Set for a write order on the selected transport. Cleared otherwise.

Bit 13 Set when an order is to be directed to transport 0. Bits 14, 15, 16 to be cleared.

Bit 14 Set when an order is to be directed to transport 1. Bits 13, 15, 16 to be cleared.

Bit 15 Set when an order is to be directed to transport 2. Bits 13, 14, 16 to be cleared.

Bit 16 Set when an order is to be directed to transport 3. Bits 13, 14, 15 to be cleared.

These bit combinations combine to give the following suggested codes for OTA 01:

For a 9 track transport (all codes in hex.)

Write record, one char/word	449X
Write record, two char/word	459X
Read record, one char/word	448X
Read record, two char/word	458X
Read and correct record, one char/word	548X
Read and correct record, two char/word	558X
Write file mark	249X
Forward one record	648X
Forward one file	248X
Backspace one record	644X
Backspace one file	244X
Rewind	002X
Select transport	800X

Note: X is the transport selection field and may have value of 1, 2, 4 or 8 for transport number 3, 2, 1 or 0 respectively.

For a 7 track transport (all codes in hex.)

Write binary record, 1 char/word	409X
Write binary record, 2 char/word	419X
Write BCD record, 1 char/word	489X
Write BCD record, 2 char/word	499X
Read binary record, 1 char/word	408X
Read binary record, 2 char/word	418X
Read BCD record, 1 char/word	488X
Read BCD record, 2 char/word	498X
Write file mark	209X
Space forward one record	608X
Space forward one file	208X
Backspace one record	604X
Backspace one file	204X
Rewind	002X
Select transport	800X

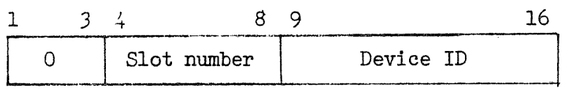
Note: X is the transport selection field and may have value of 1, 2, 4 or 8 for transport number 3, 2, 1 or 0 respectively.

5.7 OTA 02, Housekeeping setup

This OTA is used in conjunction with INA 00 (which inputs the controller's data register). Information received by the controller from the A register during the OTA is interpreted by the controller as follows:

Bit 1 If set, load the controller's data register with the current status word. The latter is defined in paragraph 5.10 below.

Bit 2 If set, load the controller's data register with the ID number. The format of the ID number is as follows:



The device ID field is $(0C)_{16}$ or $(014)_8$. The slot number field is standard and is defined further in reference B.

Bit 3 If set, load the controller's data register with the Channel number. The latter is defined in paragraph 5.4 above.

Bit 4 If set, load the controller's data register with the vector address. This is defined in paragraph 5.5 above.

The above defined bits, received by the controller as a consequence of OTA 02, are tested from left to right. If more than one bit is set, low order bits will be ignored in preference to high order bits.

5.8 OTA 03, Load and On-Line

This OTA is primarily used following an ac power failure and its function is to reload the tape and place the transport in an on-line condition. Any of the four transports may be selected by A register bits 13-16. The following codes are defined for this OTA (codes in hex.)

Power on transport	0	XX08
" " "	1	XX04
" " "	2	XX02
" " "	3	XX01

where X means the bits are ignored by the controller.

Note: As this OTA takes several seconds to perform, it should be used with discretion.

5.9 INA 00, input data register

This instruction is used to transfer the contents of the controller's data register to the central processor. The instruction should be given following an OTA 02 (which will have loaded the data register with some meaningful information).

5.10 SKS Commands

5.10.1 SKS 00, Skip if Ready

The controller will set Ready when it has loaded the data register with some information following an OTA 02. The controller will expect the central processor to issue an INA 00 to transfer that information to the A register. Ready will be cleared by the INA 00.

5.10.2 SKS 01, Skip if not busy

The controller will become busy on receipt of any OTA instruction and will remain busy until completion of that OTA. Paragraph 6.0 below indicates the duration of the busy state for various orders.

5.10.3 SKS 04, Skip if not interrupting.

The controller will cause an interrupt request to be made under the following circumstances:

a. Following the completion of any write, read or spacing operation.

b. When a transport completes a rewind operation such that the tape is positioned at load point.

c. On receipt of any illegal or undecipherable OTA instruction.

d. If an attempt is made to write tape on a transport whose file reel is write protected.

e. If an order is issued to a transport that is not on-line.

In order for the interrupt request to reach the I/O bus, the mask flip flop must be set by OCP 1514. The interrupt request must be cleared by OCP 1414 following its servicing or another false interrupt can take place.

Note: If the central processor program is servicing the magnetic tape controller using SKS Busy (as opposed to waiting for an interrupt) the controller's interrupt request flip flop should still be cleared by OCP 1414 or an immediate false interrupt could occur whenever a CP Enable Interrupt instruction is next given.

5.11 Status word

The controller maintains a status word that is relevant to the operation just completed and the transport last selected. This status word may be transferred to the A register by issuing the appropriate OTA 02 followed by an INA 00 (as detailed in paragraphs 5.7 and 5.9 above).

The bits of the status word are defined as follows:

Bit 1 Set for a vertical parity error which occurred during a read operation.

Bit 2 Set when a tape runaway condition is detected. If during a read operation no data is detected within a certain time period, the tape runaway status will be set. For a write operation, a tape runaway status will occur if the read-after-write head fails to detect the data just written within the specified time period.

Bit 3 This bit is set when a CRC error is detected during a 9 track read (or read and correct) order.

Bit 4 Set when an LRC error has been detected during a read order. For 9 track operation, it is probable that bit 3 will be set also.

Bit 5 Set for one of two reasons: (a) a false gap was detected during the record just read. Paragraph 7.2 below explains this in more detail; (b) DMX end of range occurred while reading a record before the physical end of record.

Bit 6 Uncorrectable error. Set following a 9 track read record order when the controller has determined that it will be unable to correct an error using a read and correct order. Paragraph 7.1 below expands on this problem.

Bit 7 Set when a read-after-write error is detected during a write record or write file mark order.

Bit 8 Set when a file mark is detected during any read or spacing operation.

Bit 9 Set when the selected transport is Ready to receive an order. This means it is on-line and not rewinding.

Bit 10 Set when the selected transport is on-line. This means it has power on, tape loaded, etc., and requires no further operator attention to be used.

Bit 11 Set when the selected transport has detected the end-of-tape reflective tab when moving tape in the forward direction. This sticker is placed such that 25 feet of usable tape remain on the file reel. It is the program's responsibility to ensure that the tape is not pulled off the file reel.

Bit 12 Set when the selected transport is rewinding.

Bit 13 Set when the selected transport is at load point. This means the reflective tab at the beginning of tape is under the detector.

Bit 14 Set when the selected transport is file protected. This means the file reel has had its write enable plastic ring removed.

Bit 15 Set when the controller has detected a DMX overrun condition. This is explained more fully in paragraph 6.1 below.

Bit 16 Set when an interrupt was caused by the completion of a transport rewind operation.

In summary, the status word bits are as follows:

Bit 1	Vertical parity error
2	Runaway
3	CRC error
4	LRC error
5	False gap/Insufficient DMX range
6	Uncorrectable error
7	RAW error
8	File mark detected
9	Selected transport Ready
10	Selected transport On-Line
11	" " EOT
12	" " Rewinding
13	" " Load Point
14	" " File protected
15	DMX overrun
16	Rewind interrupt

Note: The Status word is not affected by a Select OTA 01.

5.12 SKS 07, Skip if Status incorrect

This SKS allows the computer program to determine whether the status word should be further analyzed following any transport motion OTA.

The controller examines the status word following every OTA 01 (except Select) and will cause this SKS to skip unless it is equal to:

0000 0000 1100 XX00 (X for read or space orders, 0 for write orders)

(where X is a don't care).
For a Select or Rewind OTA01, this SKS will always take next instruction.
Following any other OTA (02, 03, 14, 16) the status word is not meaningful and this SKS will not skip. However, this SKS will skip if the controller receives

any illegal or undecipherable OTA.

The state of this SKS is only valid when the controller is non-busy (see para 5.10.2).

6.0 CONTROLLER TIMING

The controller will become Busy on receipt of any OTA and remain so until all action requested by the OTA has taken place. Times to perform the various OTA instructions are detailed in the following paragraphs.

6.0.1 Non-transport OTA instructions

Projected times to complete these instructions are as follows:

		μS(min)	(max)
OTA Housekeeping Setup,	Status	5.1	11.1
	ID	6.9	12.9
	Channel No.	5.7	11.7
	Vect. Addr.	6.3	12.3
OTA Channel number		2.7	8.7
OTA Vector address		3.3	9.3

The reason for the maximum and minimum times are given in paragraph 6.0.2 below.

6.0.2 OTA Setup - Rewind

The selected transport takes several minutes to rewind. However, the controller will be non-busy for all of this time except when decoding the rewind order and instructing the transport. This will take 17.1 μS minimum. This time can be extended for two basic reasons. These are as follows:

a. When the controller goes non-busy following any tape motion order, a time-out is started. The length of the time out is proportional to tape speed and is 8.3 milliseconds for 45 ips transports. At the end of the time-out, tape motion will have stopped. However, orders to the same transport are permitted to proceed during the time-out provided (a) the direction of motion has not changed and (b) the order has not changed from a read to a write or vice-versa. If these conditions are not met, the controller will store the new order for the balance of the 8.3 mS time-out and then execute the order. Hence for a rewind order, the controller may be busy for an additional 8.3 milliseconds beyond the figure of 17.1 microseconds given in paragraph 6.0.2 above.

b. When the controller goes non-busy and following the time-out for tape motion orders referenced above, the controller assumes its quiescent state. During this state it will execute a routine which tests for receipt of an OTA and then tests each transport in turn to see whether it has finished a rewind operation. This routine takes 6.0 microseconds and therefore a rewind OTA instruction can be extended by 6.0 microseconds. Also this accounts for the minimum and maximum times given in paragraph 6.0.1 above.

6.0.3 OTA Setup - Select

This non-motion transport command causes the controller to be busy for 3.0 μS minimum and 9.0 μS maximum.

6.0.4 OTA Setup - All motion commands except rewind

The controller will be busy during the entire duration of these commands and will interrupt following the end of the command. As mentioned in 6.0.2 above, a time-out of 8.3 mS is started at the time of the interrupt. For consecutive read (or write) orders, up to 16.6 mS can be saved by issuing the next order as soon as possible following the interrupt from the previous order. The time is saved by not allowing the tape to slow down or stop between orders.

The actual time to complete tape motion instructions depends on the length of the record, the density of recording and whether starting from load point or not. Typical times are as follows:

Write 800 byte, 800 bpi record	33 mS
Write 800 byte, 800 bpi record from load point	149 mS
Write file mark	83 mS

6.1 Data transfer rates

Data transfers to and from the controller occur using DMA or DMC. The controller is provided with one level of data buffering. DMA/C requests for a data transfer must be honored within the times shown in the table below or bit 15 of the status word will set indicating a DMX overrun condition.

	800 bpi	556 bpi	200 bpi
1 char/word	26.5	38.8	110
2 char/word	54.2	78.8	221

The above times are in microseconds and are for a write operation. For a read operation, add 0.9 μS to the above times.

6.2 Typical Programming Sequence

A typical sequence to write a record would be as follows: (JMP *-1's omitted)

```
Set up DMA Channel information
OTA 14, output channel number
SKS 01, wait until non-busy
OTA 16, output vector address (if non-standard address required)
SKS 01, wait until non-busy
OTA 00, output motion setup
    |
    | Wait for interrupt
SKS 04, test tape controller is interrupting
    |
    | Yes
OTA 02, Housekeeping setup to load status (or check status with SKS 07)
SKS 00, wait until Ready
INA 00, Input status
Check status and take appropriate action.
```

7.0 CONTROLLER DETAILS

7.1 CRCC information

As mentioned in paragraphs 4.3 and 4.9, a CRCC is recorded following each written record for 9 track transports. It is legitimate for the CRCC to be all zeros. Error correction is possible except under the following circumstances:

a. Errors have occurred in more than one track.

b. The "normalized" CRCC regenerated from the data plus the CRCC read from tape is equal to all zeros.

c. Character dropouts of less than three consecutive frames occurred.

7.2 Record gap detection

The controller, when reading tape, has to be able to detect the end of recorded data and the CRC and LRC characters. Figure 6 below shows that the controller searches for a 2-1/2 frame gap from the last data character. After this point, the CRCC should be detected within 3 frames and the LRCC within a further 5 frames. No data should be detected during the 16 frame period following the LRCC. If data is detected during this interval, bit 5 of the status word will be set indicating that a false gap has (probably) been detected. The consequence of this is that the tape head will not be correctly positioned in an inter-record gap. For 7 track transports, the LRCC is expected instead of the CRCC shown in Figure 6. The 16 frame gap is then started.

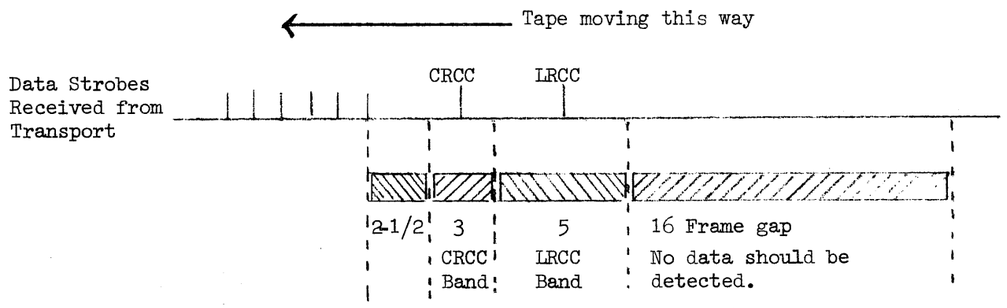


FIGURE 6

1.0 MAGNETIC TAPE TRANSPORTS

1.1 Manufacturer: Pertec Peripheral Equipment
9600 Irondale Avenue
Chatsworth, California 91311

1.2 Reference: Pertec Specification Number 103504, Revision A dated 7/26/72

1.3 Models

Model No.	Reel Size	Packing Density (Char. per Inch)	Character Transfer Rate (maximum) (KHz)	No. of Channels
8840-9-45	10.5"	800	36	9
8640-9-45	10.5"	1600	72	9
8840-75-45	10.5"	800/556	36/25	7

2.0 FUNCTIONAL OBJECTIVES

2.1 The 8 X 40 transport recording capabilities are:

2.1.1 Record 9-track 1600 cpi Phase Encoded data in ANSI and IBM compatible format or record 7- or 9-track NRZI data in ANSI and IBM compatible format.

2.1.2 The Phase Encoded or NRZI data thus recorded are capable of being reliably read by any 7- or 9-track ANSI or IBM compatible transport.

2.2 The 8 X 40 transport read capabilities are:

2.2.1 Reliably read any 1600 cpi 9-track Phase Encoded data from magnetic tape previously recorded in ANSI and IBM compatible format or any 7- or 9-track NRZI data from magnetic tape previously recorded in ANSI or IBM compatible format.

2.3 The transport provides read after write and erase capability.

3.0 GENERAL SPECIFICATIONS

3.1 The tape transport is able to record Phase Encoding or NRZI data consistent to meeting the following:

3.1.1 Phase Encoding method (9-track only). The recording method for phase encoding is defined as follows.

3.1.1.1 A "1" data bit is defined as a flux reversal to the polarity of the inter-block gap, when reading in the forward direction.

3.1.1.2 An "0" data bit is defined as a flux reversal to the polarity opposite that of the inter-block gap, when reading in the forward direction.

3.1.1.3 A flux reversal is written at the nominal mid-point between successive "1" bits or between successive "0" bits, to establish proper polarity. This flux reversal is called a Phase Flux Reversal.

3.1.2 NRZI Method (7- or 9-track): the recording method for NRZI is defined as follows.

3.1.2.1 A "1" data bit is defined as a flux reversal on tape during a character time period.

3.1.2.2 A "0" data bit is defined as the absence of a flux reversal during a character time period.

3.1.3 Density. The density of the transport is 1600 cpi or 800 bpi on 9-track, or 800/556 bpi on 7-track systems.

3.1.3.1 The density is 1600 characters per inch nominal in Phase Encoding.

(Note: Density statements in cpi are always exclusive of phase flux reversal bits.)

The transport is capable of recording at an average character spacing of 625 μ-inches ± 4 percent. This capability is measured over a 150-inch minimum length of tape which has been recorded continuously with 3200 flux reversals per inch (frpi) in any track.

3.1.3.2 The density is 800 bytes per inch nominal in NRZI 9-track systems.

(Note: Density statements in NRZI are always referred to as bytes per inch (bpi).)

3.1.4 Flux Reversal Spacing when writing 1600 cpi Phase Encoding.

(Consider the following three paragraphs in relation to each other.)

3.1.4.1 The spacing between successive data bits is nominally 625 + 75 - 98 μinches.

3.1.4.2 The spacing between data bits and an adjacent phase flux reversal is nominally 312 + 64 - 30 μinches.

3.1.4.3 The nominal spacings as listed in 3.1.4.1 and 3.1.4.2 can change but they must change simultaneously and by the same precentage not to exceed ± 10 percent total measured over 35 tape characters.

3.1.5 Total character skew for 1600 cpi Phase Encoding, and 800 bpi NRZI 9-track, and 800/556 bpi, 800/200 bpi, 556/200 bpi NRZI 7-track is as follows:

3.1.5.1 When writing 1600 cpi Phase Encoding, no data bit is displaced from any other data bit in the same character by more than 625 μinches when measured in a direction parallel to the reference edge.

3.1.5.2 When writing NRZI the maximum displacement between any two bits of a character on a tape written with all ones will be less than 225 μinches.

3.1.5.3 When reading an IBM master skew tape, IBM Part No. 432641, the maximum displacement between any two bits of the same character is less than 150 μinches.

3.1.6 Erase

3.1.6.1 Erase Direction: The tape is magnetized so that the rim end of the tape is a north-seeking pole.

3.1.6.2 Erase Width: The full width of the tape is dc erased in the direction specified in Paragraph 3.1.6.1.

3.1.6.3 The erase function, whether by the Write head or the Erase head, will ensure that the level of the read back signal amplitude is below 4 percent of the average signal amplitude at either 3200 frpi or 800 bpi.

3.2 TAPE

3.2.1 The tape used is computer grade certified at 1600 cpi. IBM Part No. 457893 or equivalent.

3.2.2 The tape width is 0.498 ± 0.002 inches and shall be nominally .0015 inches thick.

3.2.3 The tape tension is nominally 8 ounces across the heads and when winding onto the reels.

3.3 REELS

3.3.1 The transport is capable of handling up to 10.5-inch diameter reels.

3.4 TRANSPORT SPEED

3.4.1 Speed

The transport will operate at a speed of 45 ips.

3.4.2 Rewind Speed

The transport has a Rewind speed of nominal 200 ips.

3.4.3 Instantaneous Speed Variation (ISV)

The ISV is ± 3 percent maximum.

3.4.4 Long Term Speed

3.4.4.1 Long term speed variation in Forward is ± 1 percent maximum.

3.4.4.2 Long term speed variation in Reverse is ± 3 percent maximum.

3.4.5 Start/Stop

3.4.5.1 Start and stop time of the transport is 8.3 ± 0.56 milliseconds at 45 ips.

3.4.5.2 Start and stop displacement is 0.19 ± 0.02 inches to/from a speed of 45 ips.

3.4.6 Capstan and Reel Servos

The transport capstan and reel servos are capable of responding to commands given at any time during start and stop times.

3.5 PROGRAM RESTRICTION

There is no program restriction for the capstan or reel servos. However, to preserve the normal Stop-Start times and distances, and to guarantee complete erasure of the gaps, PRIME must ensure that the tape motion has ceased before changing the tape direction or Read/Write status.

3.6 MAGNETIC TAPE HEAD

3.6.1 The transport has a dual stack Read-After-Write head, with a nominal Read to Write head separation of 0.150 ± 0.005 inches.

3.6.2 The transport has a full width erase head with a nominal Erase to Write head gap separation of 0.34 inch.

3.7 PHOTO-TAB DETECTOR

3.7.1 The transport photo-tab detector is IBM-compatible and detects BOT and EOT tabs. This detector is located approximately 1.2 inches from the center of the magnetic head.

3.8 TAPE CLEANER

The transport has a block type blade tape cleaner located on the head plate capable of removing loose oxide.

3.9 ENVIRONMENTAL

3.9.1 Operating Temperature: 35°F (2°C) to 122°F (50°C) (assuming suitable tape is used).

3.9.2 Non-operating Temperature: -50°F (-45°C) to 160°F (71°C).

3.9.3 Operating Humidity: 15 to 95 percent (without condensation).

3.9.4 Altitude: Operating 0 to 20,000 feet: Non-operating 0 to 50,000 feet.

3.9.5 Shock and Vibration: The transport withstands shock and vibration encountered during normal installation and maintenance.

3.9.6 Shipping: When in the PERTEC shipping container, the unit meets the National Safe Transit specification, Project 1A, Category 1.

3.10 PHYSICAL DESCRIPTION

3.10.1	Height:	24 inches
3.10.2	Width:	19.0 inches (rack mount)
3.10.3	Depth from mounting surface: Total from front surface:	12.5 inches maximum 16.0 inches maximum
3.10.4	Mounting:	19.0 inches consistent with EIA requirements
3.10.5	Weight:	85 pounds maximum

3.10.6 A half-inch (½") filler panel is provided to make up a total height of 24.5 inches.

3.11 POWER

3.11.1 Tapped power transformer 115v/230v 300 watts maximum, 47 to 400 Hz with the following specifications.

3.11.2 115v ac Taps: 95, 100, 110, 115, 125v ac ± 10 percent.

3.11.3 220v ac Taps: 190, 200, 210, 215, 220, 225, 230, 235, 240, 250v ac + 10 percent.

3.12 ELECTRONICS

All Silicon.
The transport is designed to qualify for UL aproval.

4.0 CONTROLS AND INDICATORS

The transport provides six pushbutton indicators which are located on the front panel. Figure 4.1 shows the physical ordering of the switches.

4.1 POWER

A toggle action switch/indicator which turns ac power to the transport on and off. The indicator is illuminated when power is on and the +5v regulator is operating. When power is first applied and there is no tape in the path, the tension arms will move to their retracted position.

4.2 LOAD

Momentary action pushbutton/switch/indicator.

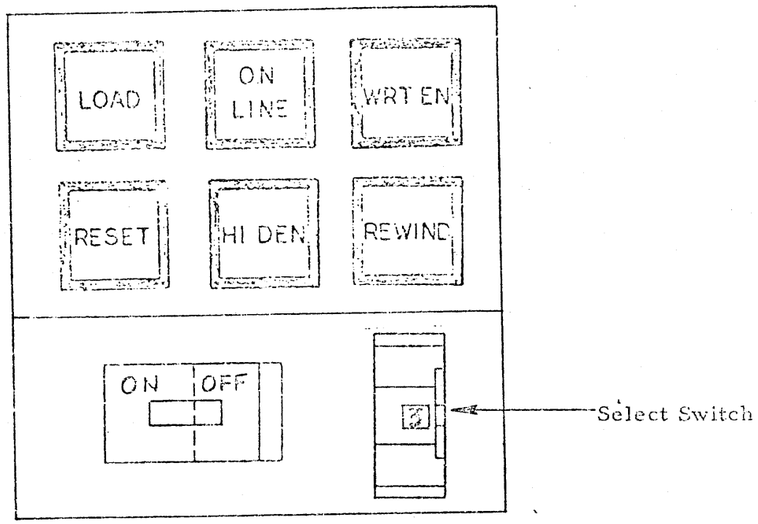


Figure 4-1. Controls and Indicators Panel

4.2.1 When load is momentarily depressed for the first time after power is switched on with the tension arms in the load position the tension arms will start moving into the operating area.

The servo systems are energized after the arms have moved more than 75 percent into the operating area. The tape will now be tensioned. The reset signal is removed after the tension arm cam is out of the normal tension arm operating area.

4.2.2 When load is momentarily depressed for the first time after power is switched on with the arms at the bottom of the operating area the servo systems are energized.

Tension is applied to the tape. The reset signal is removed.

The load switch is disabled once the second Load or Manual Rewind command has been given following power ON and can only be re-enabled by loss of tape tension or restoration of power after the Power has been off.

The indicator is lit when the BOT tab is positioned under the photosensor and:

a) The interlock is made.

b) The initial Load or Rewind command has been completed.

c) There is not a subsequent Rewind in progress. Hence, indicator lights when the transport becomes ready for use.

4.2.3 When load is momentarily depressed for the second time (which can be done before the reset signal is removed), the tape moves to and stops at Load Point after the reset signal is removed. There will be no movement if the BOT marker is already at Load Point.

4.3 REWIND

A momentary action pushbutton switch/indicator enabled only when the transport is Off-line. When REWIND is momentarily depressed, the tape moves in reverse at a nominal speed of 200 ips. On reaching the BOT tab, the Rewind drive ceases and the Load sequence is automatically entered. The BOT tab will travel past the photosensor and then move forward until the BOT tab reaches the photosensor and stops with the BOT tab at Load Point.

If already at Load Point when REWIND is depressed, the transport will go into an unload operation. This will move the tension arms close to the stops and the tape will run in reverse until tape tension is lost.

The REWIND indicator is illuminated throughout any Rewind operation including the subsequent Load sequence where relevant.

NOTE: A manual Rewind command will override the Load sequence. Thus, for example, if a Load sequence is initiated (in error) after the BOT tab has passed the photosensor, depressing the REWIND pushbutton will cause the transport to Rewind until the BOT tab is detected and then enter a Load sequence which terminates with the BOT tab at the photosensor.

4.4 ON LINE

A momentary action pushbutton switch/indicator. This switch is enabled after an initial Load or Rewind sequence has been initiated.

If the switch is depressed after an initial Load or Rewind sequence has been initiated, the transport is switched to an On-Line mode and the indicator is illuminated. In this condition, the transport is capable of receiving external commands provided it is also Ready and Selected. The transport will revert to the Off-Line mode if:

a) The RESET switch is depressed.

b) As a result of an Off-Line command (OFFC) (if transport is Selected).

c) Interlock is lost.

4.5 WRITE ENABLE

An indicator only. The indicator is illuminated whenever power is ON and a reel of tape with a Write Enable ring installed is mounted on the transport.

4.6 DATA DENSITY SELECT SWITCH

An alternate action pushbutton switch/indicator which determines the character packing density at which the read electronics operates. The indicator is marked HI DEN, and when illuminated indicates that the read electronics is conditioned to operate in the High Density mode.

If the indicator is not illuminated the transport will be in the Low Density mode. The following are the possible mode combinations:

Model	Density Combination (Character per Inch)
8840-9	800
8640-9	1600
8840-75	800/556

4.7 RESET

A momentary action pushbutton switch/indicator which stops all manual commands except Forward, Reverse, and Unload when the switch is depressed. Depressing the RESET switch when the transport is On-Line will remove the unit from On-Line operation.

4.8 FORWARD/REVERSE (Maintenance Purposes)

For maintenance purposes this 3-position toggle switch is located on the Tape Control PCBA. When the switch is in the down position, the tape will move in reverse at nominal speed. With the switch in the center position, all tape motion will cease. The up position will move the tape forward at nominal speed.

4.9 SELECT SWITCH

A rotary switch with four active positions (0 through 3) which provides addressing of selected transports. The address can only be changed when the tape unit is off-line.

5.0 TRANSPORT INTERFACE

5.1 INTERFACE INPUTS

5.1.1 Select Transport (SLT0/1/2/3)

These lines are used to select a specific tape transport for operation and only one of the four lines should be true at any one time. When a select line is true, the transport, whose rotary select switch matches the number of the select line, has all its interface drivers and receivers enabled. It is thus connected to the controller. All the lines quoted in sections 5.1 and 5.2 are gated with the select signals.

5.1.2 Synchronous Forward Command (SFC)

This is a level which, when true and the transport is Ready and On-Line causes tape to move forward at the specified speed. When the level goes false, tape motion ceases. The velocity profile shall be trapezoidal with nominally equal rise and fall times.

5.1.3 Synchronous Reverse Command (SRC)

This is a level which, when true and the transport is Ready and On-Line, causes tape to move in the Reverse direction at the specified speed. When the level goes false, tape motion ceases. The velocity profile shall be trapezoidal with nominally equal rise and fall times.

If the BOT tab is detected during an SRC, the SRC is terminated.

NOTE: The tape will not necessarily come to rest with the BOT tab in the same position as after a Load sequence. The maximum variation possible is approximately 1 inch.

If an SRC is given when the tape is at Load Point, this command is ignored.

5.1.4 Rewind Command (RWC)

This is a pulse which, if the transport is Ready and On-Line, causes tape to move in reverse at 200 ips. Upon passing BOT, Rewind shall cease and the Load sequence is automatically initiated. If already at Load Point when the Rewind command is given the command is ignored by the transport.

The velocity profile shall be trapezoidal with rise time of approximately 1 second, and fall time of approximately half a second.

The pulse is a minimum of 1 μsecond width under normal conditions.

5.1.5 Off-Line Command (OFFC)

This is a level or pulse (minimum width 1 μsecond) which resets the On-Line flip-flop to the zero state, placing the transport under manual control. It is gated only by Select in the transport logic allowing an Off-Line command to be given while a Rewind is in progress. OFFC should be separated from a Rewind command by at least 1 μsecond.

5.1.6 Write Data Strobe (WDS)

This is a pulse of minimum width 1 μsecond for each flux transition (character) to be written by the transport. The frequency of the WDS is equal to the character rate in NRZI and twice the character transfer rate in 1600 cpi PE. For NRZI the trailing edge of this pulse is used to trigger the write waveform generator in the transport. For PE the trailing edge is used to copy the PE waveform into the transport.

5.1.7 Write Data (WD) WDP, WD0-WD7 (NRZI Only)

These are levels which, if true at the time of the trailing edge of the WDS, will result in a flux transition being recorded if the transport is in the Write mode.

5.1.8 Write Data (WD) WDP, WD0-WD7 (PE Only)

These are Phase Encoded data lines which are copied into transport flip-flops on the trailing edge of WDS.

5.1.9 Set Write Status (SWS)

This is a level which must be true for a minimum period of 20 μseconds after the front edge of a SFC (or SRC) when the Write mode of operation is required.

The front edge of the SFC (or SRC) delayed is used to sample the SWS signal and set the Write/Read flip-flop in the transport to the Write state.

If the Read mode of operation is required, the SWS signal must be false for a minimum period of 20 μseconds after the front edge of a SFC (or SRC) in which case the Write/Read flip-flop is set to the Read state.

The Write/Read flip-flop can also be reset to the Read state by:

a) An RWC or OFFC.

b) Loss of interlock.

c) Switching to the Off-Line mode.

5.1.10 Overwrite (OVW)

This is a level which must be true for a minimum period of 20 μseconds after the front edge of a SFC (or SRC) when the Overwrite mode of operation is required. (In addition to selecting the Write mode.)

The front edge of the SFC (or SRC) delayed is used to sample the OVW signal and set an Overwrite flip-flop in the transport to the Overwrite state.

If the OVW signal is false for a minimum period of 20 μseconds after the front edge of a SFC (or SRC) the transport reverts to a normal Write mode of operation. (When the Write mode is selected.)

This signal is used in addition to the SWS signal when isolated records are to be updated.

5.1.11 Write Amplifier Reset (WARS) (NRZI Only)

This is a pulse of a minimum width of 1 μsecond which, when true, resets the Write Amplifier circuits on the leading edge. The purpose of this signal is to write the LRCC at the end of a record causing all channels to be erased in the IBG. This pulse will occur eight character times in 9-track systems, after the trailing edge of the WDS associated with the last NRZI data character. This pulse will occur four character times in the 7-track systems after the trailing edge of the WDS associated with the last NRZI data character.

5.1.12 Write Amplifier Reset (WARS) (PE Only)

This is a pulse of minimum width of 1 μsecond which, when true, turns off the write current in the transport. This signal is given coincident with the last flux transition of the postamble. (This signal is used only with the Overwrite.)

5.1.13 Read Threshold (RTH2) (PE Only)

This is a level which, when true, and the transport is in the Read mode, selects an extra low threshold level for the Read circuits in the transport. This level will normally be made true only when it is required to recover very low amplitude data. RTH2 must be held steady for the duration of the record.

5.1.14 Load and On-Line (LOL)

This provides the capability of remotely restoring tape tension and placing the transport back On-Line when a power failure has been experienced during operation.

The following conditions must exist before attempting to apply tape tension and placing the transport On-Line remotely.

1) Power must have returned for at least 1 second.

2) Tape must be in the path and on both reels.

3) The tension arms must be in their down position.

With the above conditions established, a true level 1.0 second in duration will apply tape tension. After a 1.0 second interval, a 1.0 μsecond pulse will place the transport On-Line.

5.2 INTERFACE OUTPUTS

The following output lines are active only when the transport is On-Line and Selected.

5.2.1 On-Line

This is a line which is true when the On-Line flip-flop is set. When true, the transport is under remote control; when false, the transport is under local control

5.2.2 Read Data (RD) RDP, RD2-RD7 for 7-track;
RDP, RD0-RD7 for 9-track

5.2.2.1 PE Output. The signals on these lines are the outputs of the 9 peak detectors, individually gated with the outputs of a threshold detector associated with each channel. The signals are a replica of the waveform used to drive the Write amplifiers.

5.2.2.2 NRZI Output. The individual bits of each data character are assembled into parallel form by a one stage deskewing register. The register outputs drive the read data interface lines RDP, RD0-RD7.

The complete character is available by sampling RDP, RD0-RD7 simultaneously on the trailing edge of the read data strobe (RDS).

5.2.3 Read Data Strobe (RDS) (NRZI Only)

This waveform is a pulse of minimum width 1 μsecond for each data character read from tape.

RDP, RD0-RD7 should be sampled simultaneously at the trailing edge or during each pulse. The pulse repetition rate (PRR) shall be on an average equal to 1/BV, where B = density and V = tape velocity.

This can vary considerably due to the combined effect of bit crowding and skew but shall not deviate more than ± 22% from the average value.

5.2.4 End of Tape (EOT)

This is a level which is true for the duration of the EOT tab. Circuitry using this output should not assume that the transitions to and from the true state are clean.

5.2.5 Transport Ready (RDY)

This is a level which is true only when all of the following conditions exist: interlocks are made; the initial Load sequence is complete; the transport is On-Line and not Rewinding. That is, the transport is ready to receive a remote command.

5.2.6 Load Point (LDP)

This is a level which is true when the interlocks are made, the BOT tab is under the photosensor, the initial Load sequence is complete, and the transport is not Rewinding. After receipt of a SFC the signal remains true until the BOT tab leaves the photosense area.

5.2.7 Rewinding (RWD)

This is a level which is true only when the transport is engaged in any Rewind operation or the Load sequence following a Rewind operation.

5.2.8 File Protect (FPT)

This is a level which is true when the following conditions exist: Power is on and a reel of tape without a Write Enable ring installed is mounted on the transport.

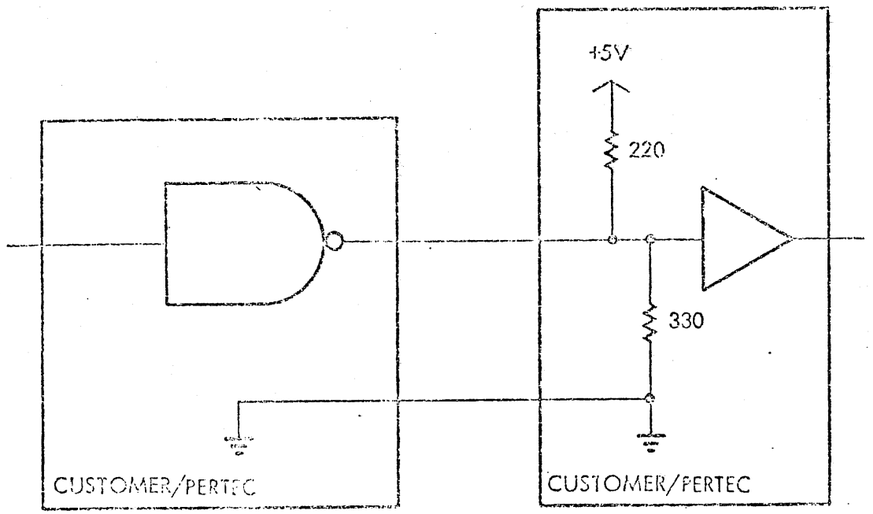
5.2.9 Data Density Indicator (DDI)

This is a level which is true only when the high density mode of operation is selected. When this line is false it indicates the low density mode has been selected.

5.3 INTERFACE ELECTRONICS SPECIFICATIONS

5.3.1 Circuits (Refer to Figure 5.1)

All drivers are DTL 944 or equivalent. All receivers are DTL 936, DTL 946 or equivalent.



ALL RESISTORS IN OHMS

Figure 5-1. Transport/Controller Interface Circuit

Table 5-1. Interface Connections

Transport Connector — 36 Pin Etched PC Edge Connector
Mating Connector — 36 Pin ELCO 00-6007-036-980-002

Connector	Live Pin	Ground Pin	Signal*
	1	2	LOAD AND ON-LINE (LOL)
	J	8	SELECT 0 (SLT0)
	A	8	SELECT 1 (SLT1)
	18	8	SELECT 2 (SLT2)
	V	8	SELECT 3 (SLT3)
	C	3	SYNCHRONOUS FORWARD Command (SFC)
	E	5	SYNCHRONOUS REVERSE Command (SRC)
	H	7	REWIND Command (RWC)
	L	10	OFF-LINE Command (OFFC)
	K	9	SET WRITE STATUS (SWS)
	B	2	OVERWRITE Command (OVW)
	T	16	READY (RDY)
	M	11	ON-LINE
	N	12	REWINDING (RWD)
	U	17	END OF TAPE (EOT)
	R	14	LOAD POINT (LDP)
	P	13	FILE PROTECT (FPT)
	F	6	DATA DENSITY INDICATOR (DDI)
	A	1	WRITE DATA STROBE (WDS)
	C	3	WRITE AMPLIFIER RESET (WARS)(NRZI Only)
	F	6	READ THRESHOLD 2 (RTH2)(PE Only)
	L	10	WRITE DATA PARITY (WDP)
	M	11	WRITE DATA 0 (WD0) } Omit for 7-Channel
	N	12	WRITE DATA 1 (WD1) } Omit for 7-Channel
	P	13	WRITE DATA 2 (WD2)
	R	14	WRITE DATA 3 (WD3)
	S	15	WRITE DATA 4 (WD4)
	T	16	WRITE DATA 5 (WD5)
	U	17	WRITE DATA 6 (WD6)
	V	18	WRITE DATA 7 (WD7)
	2	B	READ DATA STROBE (RDS)(NRZI Only)
	1	A	READ DATA PARITY (RDP)
	3	C	READ DATA 0 (RD0) } Omit for 7-Channel
	4	D	READ DATA 1 (RD1) } Omit for 7-Channel
	8	J	READ DATA 2 (RD2)
	9	K	READ DATA 3 (RD3)
	14	R	READ DATA 4 (RD4)
	15	S	READ DATA 5 (RD5)
	17	U	READ DATA 6 (RD6)
	18	V	READ DATA 7 (RD7)

* See Section III for definitions of interface functions

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MATERIAL	DWN	PRIME COMPUTER INC. NATICK, MASS.			
	CHK				
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES –DIMENSIONS ARE IN INCHES –TOLERANCES xx ± .02 xxx ± .005 ANGLES ± 1/2°	ENG.	MICRO-PROGRAMMED CONTROLLER (M2) PRODUCT SPECIFICATION			
	APPRD				
	USED ON	SCALE	SIZE	DWG. NO.	REV.
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1.0 SCOPE

This specification describes the operating characteristics and u-programming characteristics of the Micro-Programmed Controller (MPC). It is intended that this document provide sufficient information for the writer of u-programs.

2.0 APPLICABLE DOCUMENTS

PRIME I/O Bus Specification, PE-T-52 (Reference A)
PRIME 200 CPU Specification (Reference B)
PRIME Writeable Control Store, PE-TN-29

3.0 GENERAL

The Micro-Programmed Controller (MPC) consists of u-program storage (PROM) which controls the operation of device and the controller, a standard PRIME 200 I/O bus interface, with Programmed I/O, DMX, and interrupt capability, general device interfacing logic to the back edge connectors, and an area reserved for additional device specific logic if it is ever required to implement some specific controllers.

This provides an option board which with no variations to the hardware, and with only a different u-program, will meet the needs for the majority of PRIME's future device controllers. The board is capable of running with its own u-program, using an external u-program from a ROM simulator (for controller u-code development), or from an external ROM for field engineering purposes.

The MPC provides the following capabilities:

It interfaces to most TTL interfaced devices by merely inserting one of several different DIP types (with no etch changes). This implies different inventoried models or a final configuration procedure. It is capable of running in all presently defined I/O bus modes and meets all I/O bus timing specifications. It is capable of operational verification via on-board u-programs and it has the capability of displaying ROM addresses and single step control of the u-program.

It is capable of interfacing to multiple devices. No device data concurrency is provided although data interleaving can be implemented under certain circumstances. Thus, a card reader/card punch interface could be provided but an alternate read and punch on a card-by-card basis would be the most concurrency that could reasonably be achieved.

It provides the ability to satisfy some small communications controllers (up to four lines) requirements.

One back-edge connector is designed for a Field Engineering Tester. The other three may be for device connections.

The standard 20 MHZ crystal may be replaced by a crystal of lower frequency to provide particular timing that might be required.

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4.0 MPC HARDWARE SPECIFICATION

4.1 General Description

The MPC consists of (see Figure 1) a TTL Device Interface (of a general nature), PRIME I/O Bus Interface (PIO, DMX, and Interrupts), an Arithmetic Unit, a Register File (scratch pad memory), a Read Only Memory (ROM), a ROM Control Unit, and a Clock and Timing Control Unit. These units communicate via an eight bit Receive Bus and an eight bit Transmit Bus. In addition, there are various hardware assists provided such as a bit test following the Arithmetic Unit and parity checking logic at the Device Interface.

It is necessary that the Peripheral Controller Designer (μ-coder) be intimately familiar with the internal structure of the MPC so that he may effectively utilize the capabilities that it provides.

4.1.1 I/O Bus Interface

The PRIME I/O Bus Interface consists of the Standard PRIME I/O Bus Interface Logic, some registers (Data, Address, SKS, etc.) and some synchronizing logic. This is a sixteen bit interface to the I/O Bus.

4.1.2 Detailed Description

A more detailed diagram of the MPC is shown in Figure 2.

4.1.3 Device Interface

The Device Interface consists of seven registers, line drivers, line receivers, line terminations, and parity generating and checking logic. These are connected to the back-edge connectors (Device Bus) and drive or receive from twisted pair cables to the device(s).

The device interface is wired to the three 44-pin back-edge connectors (connectors C, D and E). Each connector has 22 signal and 22 ground pins providing for 22 twisted pair cables. This gives a total of 66 signal pins that are utilized for the device interface. The fourth back-edge connector is utilized by the Field Engineering Switch Panel (FEP).

The connector pins are preassigned and accommodation for particular device interface characteristics must be made by the controller designer in the cable wiring lists. The pin assignments are shown in Table I. These may be summarized by saying that there are 48 lines driven by the MPC and they are organized (enabled) into six 8-bit bytes. All of these output lines are also received by the MPC. Two additional bytes are received by the MPC (not driven). The data in the six bytes that are driven by the MPC are stored in six 8-bit registers termed Device Registers 1 through 6.

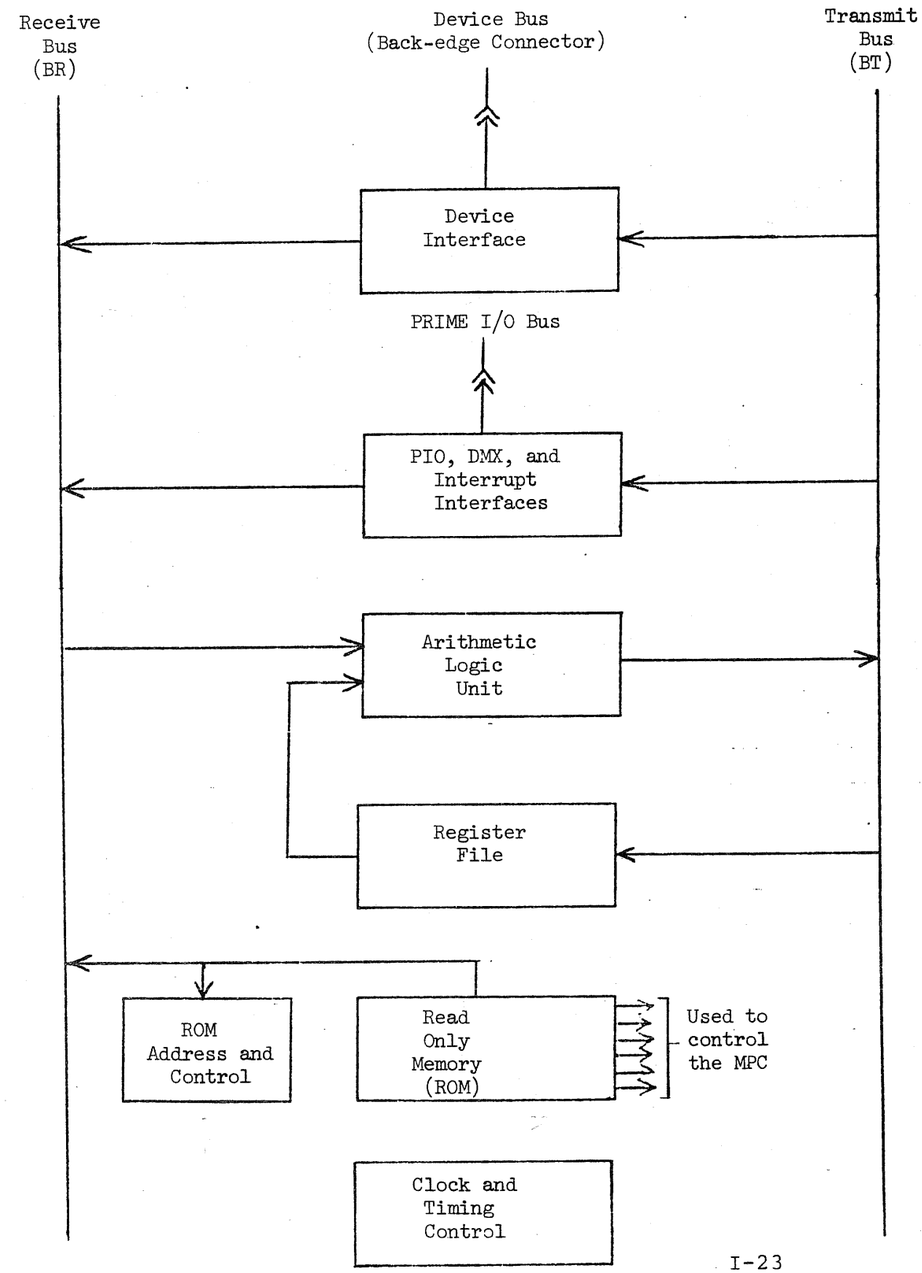

Figure 1. Block Diagram

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Figure 2. Data Flow

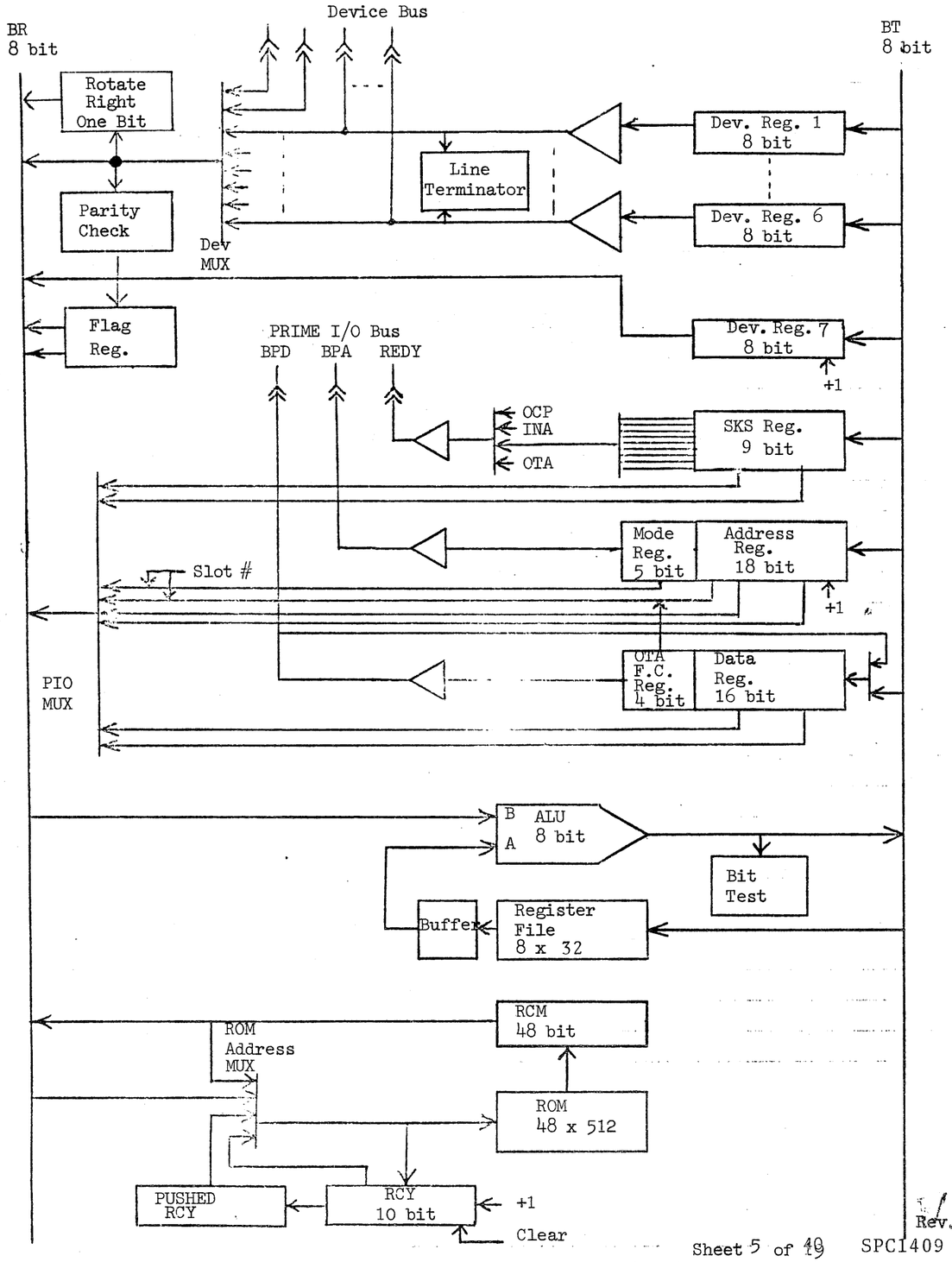

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Table I

Back-edge Connector Pin Assignments

Pin	Connector C	Connector D	Connector E	Connector F
1	Byte 1* Bit 1	Byte 3* Bit 1	Byte 5* Bit 1	TBS
3	Byte 1* Bit 2	Byte 3* Bit 2	Byte 5* Bit 2	
5	Byte 1* Bit 3	Byte 3* Bit 3	Byte 5* Bit 3	
7	Byte 1* Bit 4	Byte 3* Bit 4	Byte 5* Bit 4	
9	Byte 1* Bit 5	Byte 3* Bit 5	Byte 5* Bit 5	
11	Byte 1* Bit 6	Byte 3* Bit 6	Byte 5* Bit 6	
13	Byte 1* Bit 7	Byte 3* Bit 7	Byte 5* Bit 7	
15	Byte 1* Bit 8	Byte 3* Bit 8	Byte 5* Bit 8	
17	Byte 2* Bit 1	Byte 4* Bit 1	Byte 6* Bit 1	
19	Byte 2* Bit 2	Byte 4* Bit 2	Byte 6* Bit 2	
21	Byte 2* Bit 3	Byte 4* Bit 3	Byte 6* Bit 3	
23	Byte 2* Bit 4	Byte 4* Bit 4	Byte 6* Bit 4	
25	Byte 2* Bit 5	Byte 4* Bit 5	Byte 6* Bit 5	
27	Byte 2* Bit 6	Byte 4* Bit 6	Byte 6* Bit 6	
29	Byte 2* Bit 7	Byte 4* Bit 7	Byte 6* Bit 7	
31	Byte 2* Bit 8	Byte 4* Bit 8	Byte 6* Bit 8	
33	Byte 7** Bit 1	Byte 7** Bit 6	Byte 8** Bit 3	
35	Byte 7** Bit 2	Byte 7** Bit 7	Byte 8** Bit 4	
37	Byte 7** Bit 3	Byte 7** Bit 8	Byte 8** Bit 5	
39	Byte 7** Bit 4	Byte 8** Bit 1	Byte 8** Bit 6	
41	Byte 7** Bit 5	Byte 8** Bit 2	Byte 8** Bit 7	
43	Spare	Spare	Byte 8** Bit 8	

Even pins are ground.
* Bi-directional data capability.
** Input only capability.

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The line drivers are 7416.
drivers

Provision is also made for a component DIP to be connected to each line, to provide termination capability.

The receivers consist simply of an input to a 74151 eight to one multiplexer and the component DIP.

Thus, the two kinds of lines in the device interface are shown in Figure 3.

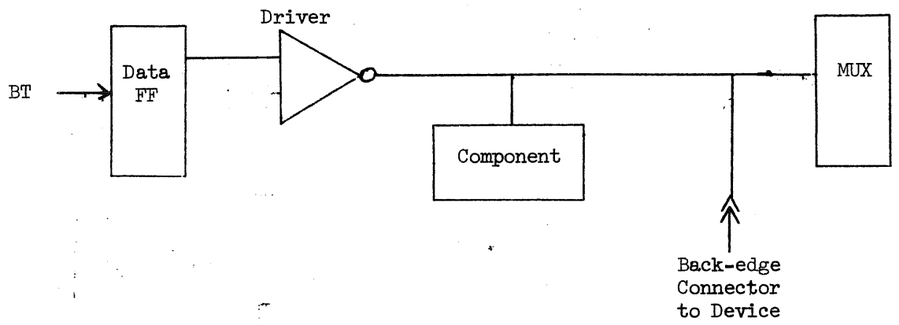

Figure 3. (a) Driven Lines (48 Lines)

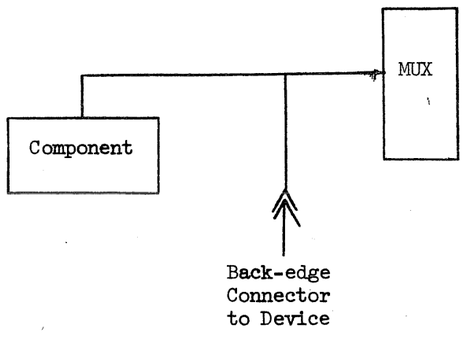

Figure 3. (b) Received Lines (16 Lines)

The use of component DIPs and drivers is optional but those used must be pin compatible with those shown in Figure 4.

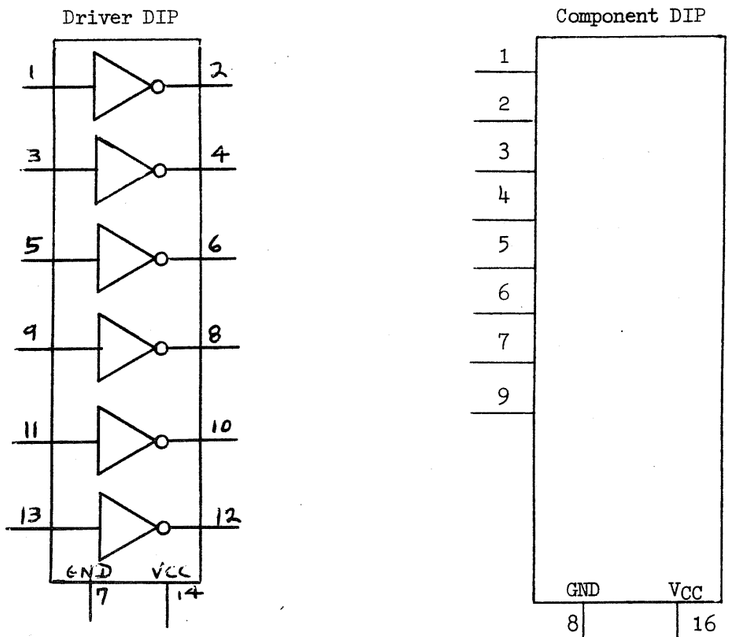

Figure 4

Several of the lines connected to the device interface have had special capabilities added in the hope of assisting the controller designer. These are described below.

(1) The parity (odd) of byte 5 and bit 7 of byte 8 (9 bits) is stored in a flip-flop whenever a leading edge is detected on bit 3 of byte 8. However, this flip-flop is not directly visible to the μ-code. The output of this flip-flop is synchronized and then can be tested at the jump net one and one-third cycles after the leading edge of bit 3 of byte 8.

An IAC will clear this flip-flop, and another IAC will set it. One must avoid clearing the flip-flop when there is a possibility of the flop being set by the interface signals to avoid ambiguous results. This is called Device Input Line Strobed Parity Flag in the μ-code documentation and should not be confused with the Device Parity Flag which comes from the Device Multiplexer.

(2) Bit 3 of byte 8 (the same signal that clocked the parity flip-flop in (1) also sets (on the leading edge) a flip-flop on every occurrence. This FF is also synchronized and can be tested with a jump condition.

An IAC can also set this FF. Another IAC clears it. Thus this jump condition can be used to either sense a positive edge on the interface line or can be used as a u-program settable and clearable flag. This is called Data Line Flag 3 in the u-code documentation.

(3) Bit 2 of byte 8 has an identical set of properties as those described in (2) above. This is called Data Line Flag 2 in the u-code documentation.

(4) Bit 1 of byte 8 has an identical set of properties as those described in (2) above. This is called Data Line Flag 1 in the u-code documentation.

(5) It should be noted that the three lines that set FF's on their leading edges (byte 8, bits 1, 2 and 3) are the output of Schmitt triggers to provide some noise immunity.

(6) In addition to the parity check described in (1) above, parity is also generated on the eight bit output of the Device Multiplexer. This parity (odd) on the eight bits may be staticized by an IAC in the Flag Register. It is testable by a jump command.

(7) If one wishes to obtain the contents of a device register on BR, one simply selects the proper device register as a source.

Two things must be considered when doing this. The first is that information enabled onto the device bus may cause undesirable action in devices connected to these lines. The second is that reflections and noise pickup on any cables connected to the device drivers may cause erroneous inputs to BR. It is recommended that one maintain the device driver outputs for two ROM cycles and only utilize the information on BR during the second ROM cycle to allow transients to die out.

(8) One may also rotate right one bit any of the Device Multiplexer outputs (a byte from a device or from a device register).

4.1.4 The standard PRIME I/O bus interface logic is discussed in detail in Reference A and will not be discussed here. The rest of the MPC I/O interface logic consists of the following parts.

a. An SKS Register
b. An Address Register
c. A Data Register
d. A Mode Line Register
e. An OTA Function Code Register
f. A Read Encoder
g. Some decoding and synchronizing logic

The use of these parts will be discussed in terms of the MPC I/O bus interactions.

The Programmed I/O (PIO) Commands for the MPC cause well-defined actions in the MPC. The defined PIO command set for the MPC is shown in Table II.

OCP's 07, 10, 15, 16 and 17 are used to control the operating modes of the MPC. They cause direct and defined hardware action and are only indirectly linked to u-code action.

OCP Acknowledge Interrupt clears the Interrupt Request F.F. in the MPC.

OCP Set Interrupt Mask sets the Interrupt Mask F.F. in the MPC. This enables the MPC to request interrupts. This F.F. is testable by the u-code. See the I/O bus specification.

OCP Clear Interrupt Mask clears the MPC's Interrupt Mask F.F. This inhibits the MPC from requesting interrupts.

OCP Initialize sets the MPC's Initialize F.F. which is testable by the u-code. The u-code is responsible for initializing most of the MPC. However, certain actions occur immediately in the MPC (i.e., via hardware) as a result of an OCP Initialize. These are:

a. Set MPC Busy
b. Clear Ready (INA and OTA)
c. Clear SKS F.F.'s 2, 3, 5, 6, 7 and 14
d. Places MPC in the PROM timing mode (300 ns cycle)
e. Causes the u-code to jump to location zero, enter RUN mode, and begin execution.
f. Clear Interrupt Mask and Request F.F.'s
g. Clear DMX Request
h. Device Registers 1, 3, 5 and 6
i. Set Initialize Flag

The result of this command is identical to what happens when Master Clear is activated.

OCP Simulator Initialize. This OCP causes the same action as OCP Initialize except that the MPC clock is put in the Simulator Timing Mode with a 400 ns cycle to allow for longer memory access time. See Figure 6-2.

OCP Stop. This command places the MPC in the Single Step Mode. The u-program may then be executed an instruction at a time by depressing the START switch on the Field Engineering Switch Panel (if connected). The only way to get the MPC back into the run mode after this OCP has been executed is via either Master Clear, OCP Initialize, or OCP Simulator Initialize.

OCP 00 sets a unique bit in the SKS Register (directly with no u-code interaction). The u-code can test the state of this bit, and any function that the controller designer wishes may be attributed to this F.F.'s being set (e.g., OCP Rewind on Mag Tape). Note that both the u-code and an OCP may set this F.F., but only the u-code may clear it. None of the other OCP's may be used.

Table II

MPC PIO Commands

Op Code Bits 1-6 / Function Code 7-10	OCP $(14)_8$	SKS $(34)_8$	INA $(54)_8$	OTA $(74)_8$
00	Set SKS 14 F.F.	Skip if INA Ready Set (H)	Input Data Register (H)	Output Data (H)
01		Skip if Not Busy (H)	--	MBS
02		MBS Skip if Set	--	MBS
03		MBS Skip if Set	--	MBS
04	--	Skip if Not Interrupting (H)	--	MBS
05	--	MBS Skip if Set	--	MBS
06	--	MBS Skip if Set	--	MBS
07	Simulator Init (H)	MBS Skip if Set	--	MBS
10	Stop Clock (H)		--	MBS
11	--		--	MBS
12			--	MBS
13			--	MBS
14	Acknowledge Interrupt (H)	MBS Skip if Set	--	Output DMA/C Channel Number
15	Set Interrupt Mask F.F. (H)		--	MBS
16	Clear Interrupt Mask F.F. (H)		--	Output Interrupt Vector
17	Initialize (H)		--	MBS

MBS = May be specified by the control designer
-- = Not defined (not useable)
H = Implemented in Hardware

Three SKS's are pre-assigned in the MPC. These allow the computer programmer to test the state of the MPC. These are SKS INA Ready, SKS Not Busy, and SKS Not Interrupting. Five other SKS's test the state of F.F.'s in the MPC which may only be set or cleared by the u-code and thus they may be assigned any meaning by the controller designer. These five SKS's skip if set. These SKS's are loaded by specifying the SKS Left Byte as the destination. SKS'02 is loaded by bit 3, SKS'03 is loaded by bit 4, etc. In addition, SKS'14 is set by OCP'00 and loaded from the u-code by bit 7 of the SKS register Right Byte.

Only one INA is implemented in the MPC (INA '00). This is Input the contents of the Data Register (in the MPC) to the CP's A register. The A register will always be cleared prior to being loaded. This INA will only be accepted by the MPC (respond Ready) if the u-code has set the INA Data Ready F.F. by an IAC. (MPC Busy has no effect on Ready.) Otherwise, the INA will not skip. The strobe resulting from an accepted INA 00 will clear the MPC's INA Data Ready F.F.

The controller designer must see that the proper information is placed into the Data Register before he sets INA Ready. This may be coordinated for various kinds of transfers (i.e., status, data, vectors, etc.) by utilizing other PIO commands to tell the MPC u-code which kind of transfer the next INA will expect.

One OTA ('00) operates in a way analogous with INA 00. That is, the MPC will only respond ready to this OTA if the u-code has set OTA Data Ready F.F. via an IAC. Otherwise the OTA will not skip. Busy has no effect on this OTA Ready condition. The strobe resulting from an accepted OTA 00 will clear the MPC's OTA Data Ready F.F.

In all other respects it is identical to the other OTA's.

All other OTA's will only be accepted by the MPC if the MPC Busy Line is false. If an OTA is accepted by the MPC, the function code of the OTA will be stored in the OTA Function Code Register by the strobe. The OTA Flag F.F. will be set. The OTA Flag will set the MPC Busy Line, thus preventing further OTA's from being accepted. The u-code alone may clear the OTA Flag F.F.

The data that accompanies the OTA (from the CP's A register) is stored into the MPC Data Register. It is the responsibility of the controller designer to preserve and interpret this data.

The data that is transferred as a result of an accepted OTA '14 must be interpreted by the controller designer as the DMA/C channel information or not used as defined in the I/O bus spec.

Likewise, the data transferred as a result of an accepted OTA '16 must be interpreted by the controller designer as the Interrupt Vector or not used as defined in the I/O bus spec.

The other 13 OTA's may be used for any purpose whatsoever. When any of these OTA's is accepted by the MPC, the Function Code is stored in the Function Code Register, the Data is stored in the Data Register and the OTA Flag and, consequently, the Busy Line are set.

The Mode Lines must all be correct during any I/O bus operation (see the I/O bus spec). Consequently the MPC forces the Mode Lines to the proper state (zeroes) during PIO operations. This is done independently of the Mode Line Register. The contents of the Mode Line Register are not altered by the MPC. The Mode Register is only used during DMX operations. For PIO and Interrupts the Mode Lines are always put in the correct state by the MPC.

4.1.5 DMX Operation

The MPC provides full DMX functionality. Either DMA, DMC or DMT transfers can occur. To perform a DMX transfer the u-coder goes through a sequence of operations as follows:

a. Test the DMX Request F.F. (end-of-data phase). If it is set, the previous transfer is still taking place. Wait, or time out.

b. When it is clear, test the End of Range F.F. If it is set, the transfer is complete. Exit this routine and clear the EOR F.F.

c. If it is not set, load the Mode Line Register (if needed); load or increment the Address Register with either the channel number in the case of a DMA or DMC transfer or a memory address in the case of a DMT transfer. Load the Data Register in the case of an input transfer or store the data that was just received in the case of an output transfer.

d. Set the DMX request F.F.

e. Go back to (a).

4.1.6 Interrupt Operation

The MPC provides standard (compatible) mode and vectored interrupt capability. The Interrupt Mask F.F. is controlled directly by OCP's 15 and 16.

The sequence of operations used to request an interrupt is to:

a. Test the Interrupt Request F.F. If it is set, an interrupt is still pending. Typically wait.

b. When the F.F. is clear, load the address register with the vector, and set the Interrupt Request F.F.

c. Test the Interrupt Request F.F. When it is cleared the interrupt has been honored and the Acknowledge Interrupt OCP has been issued.

Note that neither Override Inhibit Interrupts nor Memory Increment capability are provided by the MPC. Also note that the Mode Lines are forced to the correct state by the MPC and the Mode Register should only be used for DMX.

4.2 The Arithmetic Logic Unit (ALU) may perform any one of 32 arithmetic and logical functions on eight bit words. (See the u-code description.) One can also test the Logical Value of any one of the eight bits. The output of the ALU forms the Transmit Bus. The two inputs to the ALU are the Receive Bus (input B) and the output of the Register File (input A). Note that the ALU cannot perform the same operations on either input variable.

4.3 The Register File is a memory used for temporary storage. It is volatile so that its contents are lost when power is turned off. The Register File locations may be written into or read out of. The file is organized as 32 eight bit words. The cell addresses are 0 through 31.

4.4 The outputs of the Read Only Memory control the enabling of the data paths within the MPC on every ROM memory cycle. The ROM contains programs and subroutines which execute very much like machine language programs. The ROM is addressable up to 1024 (256 or 512 are on the MPC board) 48 bit words. The output of the ROM is stored in RCM to provide stable glitch-free outputs.

These u-programs are unique to each type of MPC based controller. They are programmed into the MPC by "blowing" Programmable Read Only Memory (PROM) DIPs, and inserting these onto the MPC board. The ROM Address MUX and RCY acts as a memory interface to the ROM, specifying the address of the next ROM location to be fetched and providing the appropriate timing. The Pushed RCY Register provides a one deep stack for fast subroutining. One may Push onto Pushed RCY or Pop Off of Pushed RCY via independent action codes in the u-code.

4.5 The Flag Register bit assignments are as follows:

	Bit	
(MSB) Right Byte	1	Device Parity F.F. (Even) for Input
	2	Interrupt Mask F.F.
	3	DMA/C End of Range F.F.
	4	Normal Mode F.F.
	5	Strobed Device Parity F.F. (Odd) for Input
	6	Device Input Line F.F. 1 Trailing Edge Trigger
	7	Device Input Line F.F. 2 Trailing Edge Trigger
	8	Device Input Line F.F. 3 Leading Edge Trigger
Left Byte	1	Initialize Flag
	2	OTA Flag
	3	SKS Flag (Set by OCP'00, Loaded by SRR, bit 7)
	4	u-Code Busy Flag
	5	INA (00) Data Ready Flag
	6	DMX Request Flag
	7	Interrupt Request Flag
	8	OTA (00) Data Ready Flag

4.6 Two additional flags (5 and 6) are provided. These may be set or cleared by IAC and their condition tested by a jump.

The Busy condition which determines the acceptance of OTA's is the Logical OR of the u-code Busy Flag, the Initialize Flag, and the OTA Flag.

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5.0 MPC u-CODE SPECIFICATION

The u-code resides in the ROM. The ROM is addressable up to 512 words. A ROM word is 48 bits long and is organized into fields, each of which performs a specific function. It is useful to note that the definitions and actions of the u-code relate directly to the structure of the MPC hardware and Figure 2 will be a visual aid that the u-coder needs in order to write u-code for the MPC.

5.1 u-Code Format

The basic u-code format is shown in Figure 5. The detailed u-code description is given in Table III. A complete description of these fields follows.

The u-code word is read out of ROM from the addressed location and stored in the RCM register on every ROM cycle. It is the output of the RCM that controls the MPC.

5.2 MPC u-Code Assembler

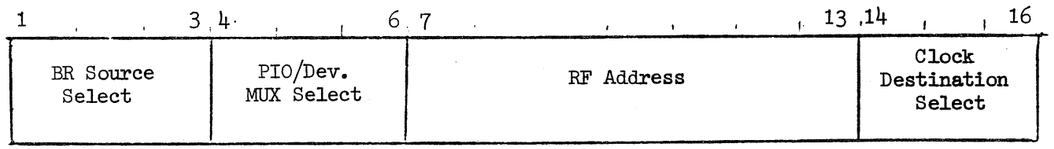
A description of the MPC u-code Assembly Language Syntax is given in section 7.9.

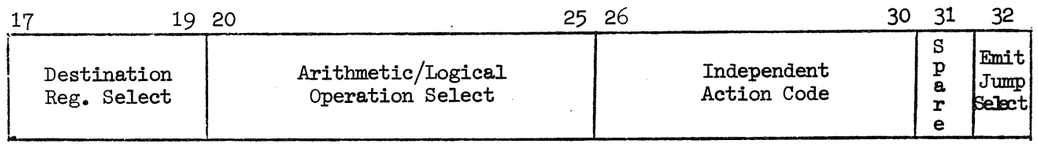
A summary of the mnemonics used is given in Table III.

	USED ON	SCALE	SIZE	DWG. NO.	REV.
	NEXT ASSY	SHEET 15 OF 40	A	SPC1409	I

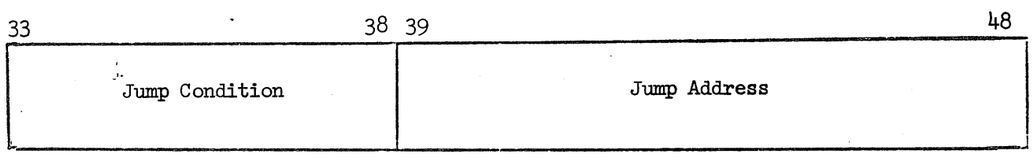
PDF-005

Figure 5. μ-Code Format

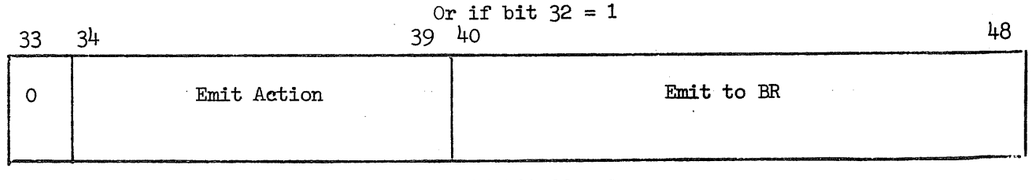




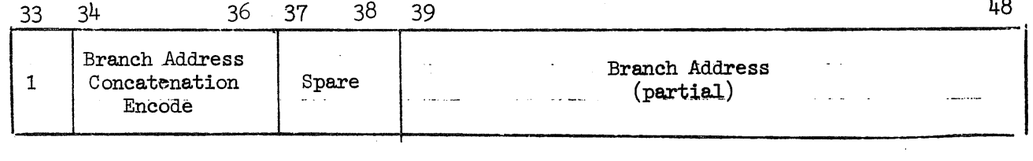
If bit 32 = 0



Or if bit 32 = 1



Or if bit 32 = 1



ROM Bits	Field	Description	Mnemonic(s)
1-3	A	Receive Bus (BR) Source Select	
		0 RCM (bits 41 thru 48)	RCM
		1 Dev MUX	See Field B
		2 PIO MUX	See Field B
		3 Flag Reg-R.B.	FRR
		4 Dev MUX Rotated Right	See Field B
		5 Dev Reg 7	DR7
		6 --	-
		7 Flag Reg-L.B.	FRL

ROM Bits	Field	PIO and Dev MUX Source Select	Dev MUX	PIO MUX	Dev MUX Rotated Right
4-6	B	0 Dev Byte 1 and Data Reg R.B.	DR1	DRR	DR1RR
		1 Dev Byte 2 and Add Reg R.B.	DR2	ARR	DR2RR
		2 Dev Byte 3 and SKS Reg R.B.	DR3	SRR	DR3RR
		3 Dev Byte 4 and Mode Reg*	DR4	MR	DR4RR
		4 Dev Byte 5 and Data Reg L.B.	DR5	DRL	DR5RR
		5 Dev Byte 6 and Add Reg L.B.	DR6	ARL	DR6RR
		6 Dev Byte 7 and SKS Reg L.B.	DB7	SRL	DB7RR
		7 Dev Byte 8 and OTA F.C. Reg**	DB8	OFC	DB8RR

*

1	2	3	4	5	6	7	8
BPCSS01	BPCSS02	BPCSS03	INMOD (4)	0	1	2	3
Slot #				Mode Reg			

**

1	2	3	4	5	6	7	8
BPCEXS1	BPCEXS2	99	00	7	8	9	10
Slot #		High Order Address Bits		OTA Function Code Bits			

Note: R.B. = Right Byte (bits 9-16)
L.B. = Left Byte (bits 1-8)

TABLE III. u-Code Description - Assembly Language Mnemonics

Table III. u-Code Description (continued)

ROM Bits	Field	Description	Mnemonic
7-13	C	Reg File (RF) Address	RF nn
		If bit 7 = 0 the RF Address comes from bits 9-13. Bit 8 is not used.	
		If bit 7 = 1 the RF Address comes from the low order 6 bits of Dev Reg 7. (8-13 are not used.)	
14-16	D	Clock Destination Register Select (always Clock RCM).	
		No Bit set - Clock RCM Only	-
		Bit 14 set - Clocks PIO Registers	See Field E
		Bit 15 set - Clocks Dev Registers	See Field E
		Bit 16 set - Clocks R.F.	RF nn
		Any combination of bits is valid.	

ROM Bits	Field	Destination Register Select	Dev Reg	PIO
17-19	E	0 Data Reg R.B.	-	DRR
		1 Dev Reg 1 & Add Reg R.B.	DR1	ARR
		2 Dev Reg 2 & SKS Reg R.B.	DR2	SRR
		3 Dev Reg 3 & Mode Reg	DR3	MR
		4 Dev Reg 4 & Data Reg L.B.	DR4	DRL
		5 Dev Reg 5 & Add Reg L.B.	DR5	ARL
		6 Dev Reg 6 & SKS Reg L.B.	DR6	SRL
		7 Dev Reg 7 OTA FC & HO Add*	DR7	OFC

*

1	2	3	4	5	6	7	8
		99	00	7	8	9	10
Not Used		High Order Address Bits		OTA Function Code Bits			

ROM Bits	Field	Arithmetic Operation
20-25	F	
20-21		0 Arithmetic Mode C = 0
		1 Arithmetic Mode C = 1
		2 Arithmetic Mode C = Carry Out of ALU
		3 Logical Mode

Note: C = Carry into low order ALU bit

Table III. u-Code Description (continued)

ROM Bits	Field	Description	Mnemonic
20-25	F	Arithmetic and Logic Unit	
		Logical Modes	
		0 A	RF nn
		1 A∧B	AND
		2 A∧B--*	-
		3 0	CON ZERO
		4 AVB	OR
		5 B	BR
		6 A∀B	XOR
		7 A--∧B	-
		8 AVB--	-
		9 --(A∀B)	-
		A --B	BRN
		B --(AVB)	NOR
		C 1 (Logical)	ONE
		D A--VB	-
		E --(A∧B)	-
		F --A	RFN nn
		- - - OR - - -	
		Arithmetic Codes (add 1 if Carry = 1)	
		0 A	INC RF nn (C = 1)
		1 (A∧B--)+A	-
		2 A∧B+A	-
		3 A+A=2A	LS
		4 AVB	-
		5 (AVB--)+(AVB)	-
		6 A+B	PLUS
		7 A+(AVB)	-
		8 AVB--	-
		9 A-B-1	MINUS (C = 1)
		A (A∧B)+(AVB--)	-
		B A+(AVB--)	-
		C -1	CON MINUS 1
		D (A∧--B)-1	-
		E A∧B-1	-
		F A-1	DEC RF nn

Note: -- ≡ NOT
A = Register File
B = Receive Bus

Table III. u-Code Description (continued)

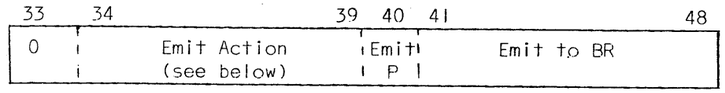
ROM Bits	Field	Description	Mnemonic
26-30	G	Independent Action Codes	
		0 Jump to Zero	JZ
		1 Pop (Jump to Pushed RCY)	POP
		2 Push (Load Pushed RCY with RCY)	PSH
		3 +1 to Add Reg	IAR
		4 +1 to Dev Reg 7	IDR7
		5 Set INA Data Ready F.F. (INA00)	SIRDY
		6 Clear u-Code Busy F.F.	CB
		7 Clear OTA Flag	COF
		8 Clear Initialize Flag	CIF
		9 Set OTA Data Ready F.F. (OTA00)	SORDY
		A	-
		B Load Input Dev Parity into Flag	SIPF
		C Set Flag 5	SF5
		D Set Flag 6	SF6
		E Set u-Code Busy F.F.	SB
		F Store Condition Codes	SCC
		10 NOP	NOP
		11 Set Interrupt Req F.F.	SIRQ
		12 Set DMX Req F.F.	SDRQ
		13 Clear DMX EOR F.F.	CDEOR
		14 Clear Dev Line Input Flag 1	CF1 (CDI1)
		15 Clear Dev Line Input Flag 2	CF2 (CDI2)
		16 Clear Dev Line INput Flag 3	CF3 (CDI3)
		17 Clear Dev Line Parity Flag	CF4 (CDIP)
		18 Set Dev Line Input Flag 1	SF1 (SDF1)
		19 Set Dev Line Input Flag 2	SF2 (SDF2)
		1A Set Dev Line INput Flag 3	SF3 (SDF3)
		1B Set Dev Line Input Parity Flag	SF4 (SDFP)
		1C Clear Flag 5	CF5
		1D Clear Flag 6	CF6
		1E Clear DMX Req F.F.	CDRQ
		1F	-
31		Spare	
32	H	Emit/Jump Select	
		0 = Conditional Jump implies that field J is the Jump condition and field K is the Jump Address	JUMP ON (NOT)
		1 = Emit or Branch. Bits 33-48 are further decoded.	EMIT, BRANCH

Table III. u-Code Description (continued)

ROM Bits	Field	Description	Mnemonic
33-38	J	Jump Conditions (if bit 32 = 0)	
33		If bit 33 is a 0, the MPC will Jump when the addressed condition is False. If bit 33 is a 1, the MPC will Jump when the addressed condition is True.	
34-38		0 True	T
		1	-
		2 SKS Flag (OCPoo)	SKSF
		3 OTA Flag	OTAF
		4 OCP Initialize Flag	INTF
		5 Carry Out of Add Reg bit 1	ARCO
		6	-
		7 OTA Data Ready Set (OTAOO)	ORDY
		8 Bit Test Condition Code SEt	CCBT
		9	-
		A	-
		B	-
		C	-
		D	-
		E	-
		F	-
		10 Carry Out of Dev Reg 7 bit 1	DR7CO
		11 Flag 5	F5
		12 Flag 6	F6
		13 Carry Out of ALU Cond. Code Set	CCACO
		14 ALU High Order bit Cond. Code Set	CCAHO
		15 DMX Req Set (end of Data phase)	DRQDP
		16 Interrupt Req Set (before mask)	IRQ
		17 INA Data Ready Set (INAOO)	IRDY
		18 Input Parity Even	PIE
		19 ALU equal zero Cond. Code Set	CCAEZ
		1A End of Range	EOR
		1B ALU less than or equal zero Cond. Code Set	CCALEZ
		1C Device Input Line Flag 1 Set	F1 (DIF1)
		1D Device Input Line Flag 2 Set	F2 (DIF2)
		1E Device Input Line Flag 3 Set	F3 (DIF3)
		1F Device Input Strobed Parity Flag Set	F4 (DIFP)

Table III u-Code Description (continued)

ROM Bits	Field	Description	Mnemonic
39-48	K	Jump Address from ROM (if Bit 32 = 0)	
33-48	J'	If ROM bit 32 = 1, then bits 33-48 are decoded as:	
33		If Bit 33 = 0, Emit or Bit 33 = 1, Unconditional Branch If Emit, ROM Bits 34 thru 48 are interpreted af follows:	



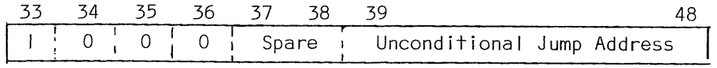
Emit P (Parity) is not implemented in current MPC.

34-39	J'	Emit Action if bit 32 = 1 and bit 33 = 0 bits 34-39 are interpreted as follows:	
34-36		Set the Bit Test Condition Code if bit at the output of the ALU specified by these 34-36) ROM bits is a one, and the Set Condition Code Independent Action Code is given:	
		0 ALU bit 1 = 1	ACT 1
		1 ALU bit 2 = 1	ACT 2
		2 ALU bit 3 = 1	ACT 3
		3 ALU bit 4 = 1	ACT 4
		4 ALU bit 5 = 1	ACT 5
		5 ALU bit 5 = 1	ACT 6
		6 ALU bit 7 = 1	ACT 7
		7 ALU bit 8 = 1	ACT 8

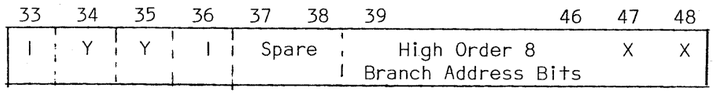
Table III. u-Code Description (continued)

ROM Bits	Field	Description
37-39		TBS

If Bit 33 = 1, RCM Bits 34-48 are interpreted as follows:

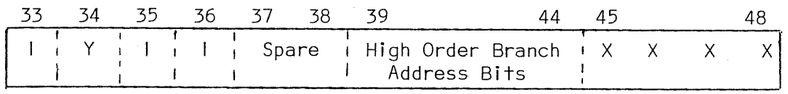


or Four Way Branch



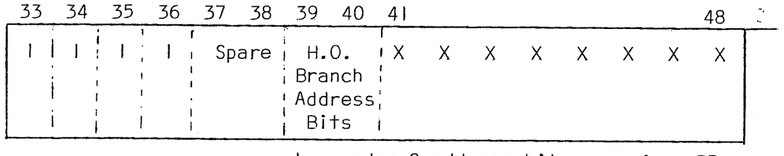
The Low order two address bits come from BR

or Sixteen Way Branch



Low order four address bits come from BR

or 256 Way Branch



Low order 8 address bits come from BR

In other words, bits 34, 35 and 36 specify which Branch address bits come from RCM and which from BR. If the Y bits are not zero, then other concatenations of address occur. These are shown in Table IV.

Table IV

RCM Bits			Branch Address Bit Source			
34	35	36	High Order	--	--	Low Order
0	0	0	RCM 39, 40	RCM 41-44	RCM 45, 46	RCM 47, 48
0	0	1	RCM 39, 40	RCM 41-44	RCM 45, 46	BR 7, 8
0	1	0	RCM 39, 40	RCM 41-44	BR 5, 6	RCM 47, 48
0	1	1	RCM 39, 40	RCM 41-44	BR 5, 6	BR 7, 8
1	0	0	RCM 39, 40	BR 1-4	RCM 45, 46	RCM 47, 48
1	0	1	RCM 39, 40	BR 1-4	RCM 45, 46	BR 7, 8
1	1	0	RCM 39, 40	BR 1-4	BR 5, 6	RCM 47, 48
1	1	1	RCM 39, 40	BR 1-4	BR 5, 6	BR, 7, 8

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6.0 MPC TIMING

Figure 6-1 shows the internal timing of the MPC. TCLKC+, TCLKL, TCLK1, TCLK2, and TCLK3 are the basic timing pulses. All other timing signals are derived from these.

6.1 Detailed Timing Description

The first clock (TCLK1) performs the following:

(a) Load RCM at the beginning of every cycle (300 ns). This staticizes the ROM output and changes the control outputs throughout the MPC.

(b) RCY is loaded on every cycle.

(c) Staticize all inputs to the jump net.

6.2 The second clock (TCLK2) performs the following functions:

(a) It increments RCY (adds one to RCY). This is so that the next sequential ROM cell will be accessed on the next cycle if no jumps or branches occur.

(b) The independent action code (IAC) (if any) output appears. Some IAC's cause action at this time. Others cause action on the trailing edge of the IAC output. Still others have other timing. These are shown separately in Figure 6-1.

The middle of the second clock causes the Register File output to occur and these are latched at the end of the second clock time.

The middle of the third cycle causes:

(a) The end of the IAC output causing it to go high (if there was one). This would cause the Pushed RCY Register (PRY) to be loaded if that IAC had been coded.

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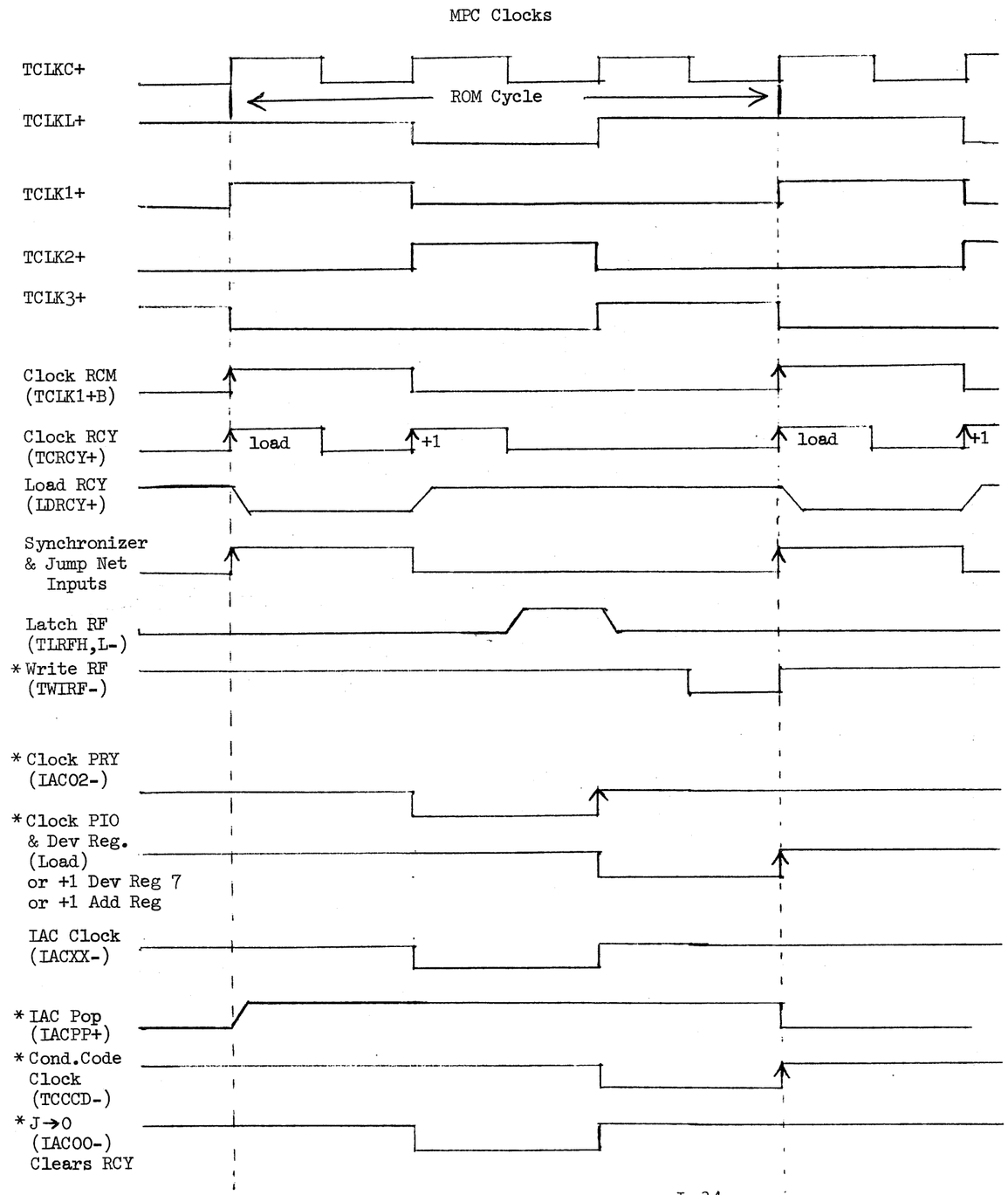

Figure 6-1

* Does not happen every cycle.

(b) The Register File cell that was addressed will be written into if that was specified as a destination register.

The end of the third cycle (at the same time as the beginning of the next cycle) causes:

(a) The device Register and/or the PIO Register to be loaded if they are specified as destination registers.

(b) Device Register 7 or the Address Register will be incremented if that IAC is specified. This will occur instead of that Register being loaded if both are specified.

Then the process repeats.

6.3 ROM Simulator and External ROM Timing

If the PROM/SIM switch in the clock logic is placed in the SIM position or OCP Simulator Initialize is issued the basic clocks in the MPC change as shown in Figure 6-2. That is, TCLK3 doubles in length. This allows 100 nanoseconds more time for the external memory access (ROM, PROM, ROM Simulator, or Writable Control Store) to take place.

Thus the MPC's cycle time increases 33%.

6.4 Single Cycle Timing

If the RUN/Single Cycle switch in the clock logic is placed in the Single Cycle position, or OCP Stop Clock has been issued, the basic clocks in the MPC suspend every cycle until the Start switch is pushed. The clock suspends at the end of TCLK2. See Figure 6-3.

7.0 MPC μ-PROGRAMMING RULES

7.1 Register Loading

(a) If both the loading of a Register (as a destination) and the incrementing of a Register are specified, the Register will be incremented by one (the previous contents of the register +1) not loaded.

(b) Up to three destination registers may be specified in the same μ-instruction. However, there are certain restrictions.

(1) The same cell in RF whose address is specified will be loaded if RF is specified as a destination register. The output of RF will not change until the middle of the next cycle.

(2) A device register and a PIO register may be loaded if both are specified as destination registers but only in pairs as specified in field E. For example, one could not load both Device Register 3 and the SKS Register with the same μ-instruction.

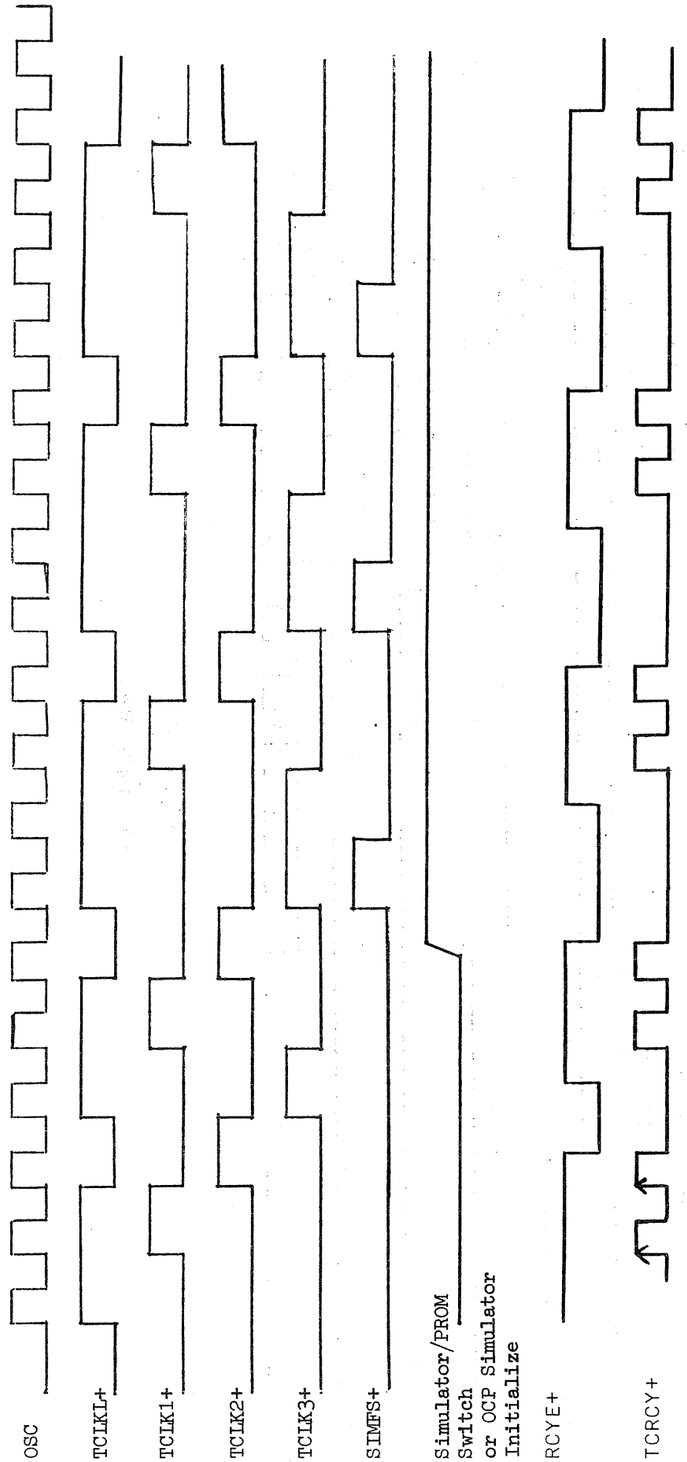

Figure 6-2
MPC
Simulator Mode Timing

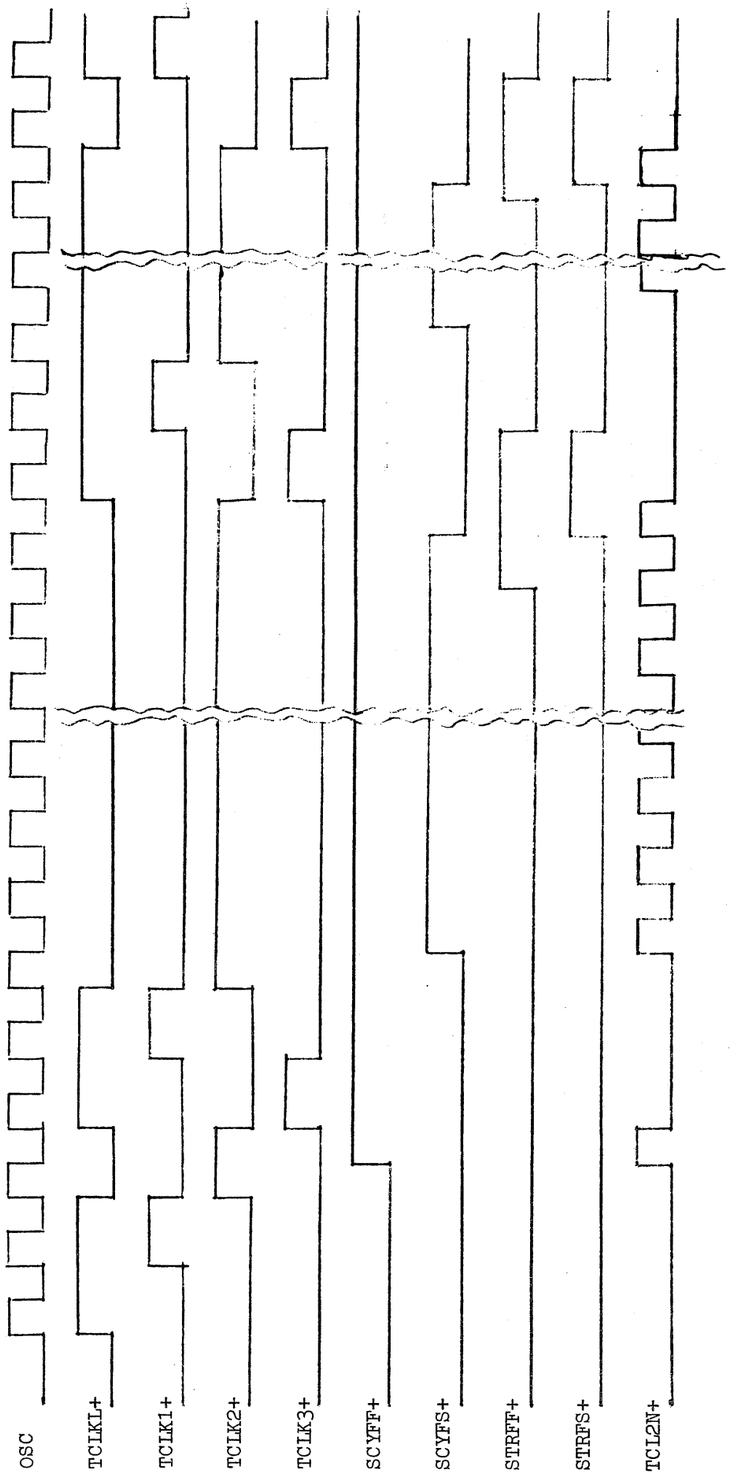

Figure 6-3
MPC Single Step

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7.2 Source Select

(a) If either the Device MUX or the PIO MUX is specified as the source of BR, field B must specify what the specific BR source is.

7.3 Arithmetic Operations

(a) The A input of the ALU is always the output of the Register File. The B input of the ALU is always what is enabled to BR.

(b) The carry out of the high order nibble (4 bits) of the ALU, the high order bit of the ALU, the ALU equals zero condition, and the result of the bit test will only be stored in the condition code register at the end of the current cycle if the set condition code IAC is specified in the current instruction. Any of the condition codes may then be tested any number of times in any succeeding cycles, including the next cycle in which the set condition code IAC is specified.

7.4 Independent Action Codes

(a) Only one IAC may be specified in any single u-instruction.

(b) All IAC's will take precedence over any conflicting commands except for the jump to zero IAC (see (c)).

(c) The jump to zero IAC will not take place if a conditional jump is successful or if a branch is specified, i.e., ROM bit 32 = 1 and ROM bit 33 = 0. If a condition jump is not successful, no branch is specified and a jump to zero IAC is specified, the jump to zero will occur.

(d) IAC's Clear OTA Flag and Clear Initialize Flag should only be done when u-code Busy is set.

7.5 Conditional Jumps

The jump net starts to stabilize at the beginning of a ROM cycle. It must result in a stable address to the ROM by the end of the cycle. Thus no jump net inputs are allowed to change after the beginning of a cycle and must remain stable through the end of the cycle.

This implies that either the tested condition is synchronous with the MPC or that a synchronizer is used. Where a two F.F. synchronizer is used, up to one and one-third ROM cycle of delay can result from the time that the condition occurs until it can cause a jump.

The worst case condition is that the condition to be tested just comes up at the first FF clock of the synchronizers (i.e., the end of the second clock). The end of third clock sets the second FF and starts the jump net settling. The settling takes one cycle. If the condition being tested occurs any later than the end of the second clock in the instruction prior to the jump u-instruction, the MPC will not jump. See Figure 6-4.

Location zero of the u-code can not contain a jump on (not) Initialize Flag.

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The conditions that must by synchronized in this manner are:

1	
2	SKS Flag (OCP 00)
3	OTA Flag
4	OCP Init Flag
7	OTA Ready Set (00)
15	DMX Req Set (Data Phase)
16	Interrupt Req Set
17	INA Ready Set (00)
18	Input Parity Even
1A	End of Range Set
1C	Device Input Line 1 Flag Set
1D	" " " 2 " "
1E	" " " 3 " "
1F	" " Strobe Parity Flag Set

IAC's affecting the above conditions will be guaranteed to cause the action so that the synchronizer will work on the current cycle, i.e., before the end of the second clock.

All of the other jump conditions are the result of a previous u-code operation and are guaranteed to be stable in the jump net.

In summary, in order to jump on a condition that must be synchronized by the MPC (listed above) the condition must have occurred prior to clock three of the previous cycle.

All other conditions may be the results of the previous u-instructions. Thus:

```
Add +1 to RF7 - Set Condition Code
Jump on Condition Code Set

IAC Clear OTA Flag
Jump on OTA Flag
Jump* -2
```

are valid u-instruction sequences.

7.6 (a) If an Emit is specified it will only be used if RCM is specified as the source of BR.

(b) In order to set the Bit Test Condition Code it is necessary to specify which bit is to be tested in the Emit Action Field. That is, one must specify the ALU operation to be performed, specify a Set Condition Code IAC, and specify an Emit and an Emit Action in the same u-instruction. The jump on the bit test condition code can be done in any subsequent u-instruction.

7.7 The various branches that may be performed will always take place instead of a jump to zero IAC if both are specified in the same u-instruction.

7.8 When writing a C.P. program using the MPC, one must take care not to cause the MPC to alter the Address Register or the Mode Register prior to completing an interrupt or DMX transfer.

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7.9

GENERAL

THIS DOCUMENT DESCRIBES THE LANGUAGE PROCESSED BY THE MPC MICRO-CODE ASSEMBLER. THE ASSEMBLER CONSISTS OF A MACRO PACKAGE THAT ALLOWS THE STANDARD PRIME ASSEMBLER TO ASSEMBLE CODE FOR THE MICROPROGRAMMED CONTROLLER.

APPLICABLE DOCUMENTS

-- MICRO-PROGRAMMED CONTROLLER PRODUCT SPECIFICATION (PE-T-53)
-- PRIME MACRO ASSEMBLER MANUAL (SECTIONS ONE AND TWO)

DESCRIPTION LANGUAGE ELEMENTS

A MODIFIED BNF TYPE LANGUAGE IS USED IN THIS DOCUMENT TO DESCRIBE THE MPC ASSEMBLY LANGUAGE. THE BASIC FORMS OF THIS LANGUAGE ARE:

[...]	ITEMS BETWEEN SQUARE BRACKETS ARE OPTIONAL
↑	SEPARATES ALTERNATIVE CHOICES
<...>	METASYMBOL, ITEM FITTING THE DEFINITION OF THE SYMBOL MUST BE SUBSTITUTED FOR THE SYMBOL
<...> ::=	METASYMBOL DEFINITION.

PROGRAM STRUCTURE

PROGRAMS WILL BE STRUCTURED AS FOLLOWS:

-- INTRODUCTORY COMMENTS
-- AN INSERT STATEMENT OF THE FOLLOWING FORM:
   $INSERT MPC
   THIS STATEMENTS DIRECTS THE ASSEMBLER TO READ AND STORE THE MPC MACRO DEFINITIONS
-- VERSION IDENTIFICATION (SEE IDNT MACRO DESCRIPTION)
-- PROGRAM TEXT (SEE MPC AND ORG MACRO'S)
-- END STATEMENT

IDNT MACRO

THE IDNT MACRO IS USED TO SPECIFIY A VERSION IDENTIFICATION. THE FORMAT OF AN IDNT MACRO CALL IS:

```
      IDNT   (<STRING>),(<STRING>),...

<STRING> := A STRING OF UPTO 30 CHARACTERS.  THE
            STRING MAY NOT INCLUDE SEMICOLONS (;),
            COLONS (:), OR PARENTHESIS.
```

UPTO TEN STRINGS MAY BE SPECIFIED, BUT ONLY THE FIRST 60 CHARACTERS WILL BE USED. THE IDENTIFICATION PRODUCED WILL CONSIST OF THE STRINGS (EXCLUDING SURROUNDING PARENTHESIS) SEPERATED BY SPACES. FOR EXAMPLE,

```
      IDNT   (MPC TEST),(  JULY 5, 1973)
```

WOULD PRODUCE THE IDENTIFICATION:

ID: MPC TEST JULY 5, 1973

ORG MACRO

THE ORG MACRO IS USED TO CHANGE THE ASSEMBLER PROGRAM COUNTER. THE FORMAT IS:

```
      ORG    <EXP>
```

WHERE <EXP> IS EVALUATED AS AN ASSEMBLER EXPRESSION AND USED AS THE NEW PROGRAM COUNTER.

MPC MACRO

THE MPC MACRO IS USED TO SPECIFY ONE MPC INSTRUCTION WORD. THE PERMISABLE FORMS OF MPC MACRO CALLS ARE AS FOLLOWS:

```
<MPC INSTRUCTION> := [<LABEL>] MPC <OPERATION>
```



```
<OPERATION> := <BASIC OP> [<IAC> [<ACT SPEC>]]

<BASIC OP> := <TRN OP>↑<ALU OP>↑<INC OP>↑<DEC OP>↑
              <NOT OP>↑<CON OP>↑<NOP OP>

<TRN OP> := TRN <GEN SOURCE> => <GEN DEST>

<ALU OP> := <RF SPEC> <OP> <BR SPEC> [+ <ALUCS>]
            => <GEN DEST>

<INC OP> := INC <RF SPEC> => <GEN DEST>

<DEC OP> := DEC <RF SPEC> => <GEN DEST>

<NOT OP> := NOT <GEN SOURCE> => <GEN DEST>

<CON OP> := CON <CON SPEC> => <GEN DEST>

<CON SPEC> := ZERO↑MINUS1

<NOP OP> := NOP

<GEN SOURCE> := <RF SPEC>↑<BR SPEC>↑ NOP

<RF SPEC> := RF <EXP>↑RFDR7

<BR SPEC> := <DM SPEC>↑<PM SPEC>↑<RCM SPEC>↑
             FRR↑<DMRR SPEC>↑DR7↑FRL↑
             0↑1↑2↑...↑7

<DM SPEC> := DR1↑DR2↑DR3↑DR4↑DR5↑DR6↑
             DB7↑DB8

<DMRR SPEC> := DR1RR↑DR2RR↑DR3RR↑DR4RR↑
               DR5RR↑DR6RR↑DB7RR↑DB8RR

<PM SPEC> := PM <PMS>↑<PMS>

<PMS> := DRR↑ARR↑SRR↑MR↑DRL↑ARL↑SRL↑
         OFC↑0↑1↑2↑...↑7

<RCM SPEC> := RCM↑RCM = <EXP>

<OP> := <LOGOP>↑<AOP1>↑<AOP2>

<LOGOP> := RF↑AND↑ZERO↑OR↑BR↑XOR↑BRN↑
           NOR↑ONE↑RFN
```

```
<AOP1> :: PLUS↑LS↑SUB↑0↑1↑2↑...↑F                (ALUCS may be specified)

<AOP2> :: MINUS                                  (ALUCS may not be specified)

<ALUCS> :: 0↑1↑C↑L

<GEN DEST> :: NOP↑<DEST SPEC>↑
              (<DEST SPEC>[,<DEST SPEC>[,<DEST SPEC>]])

<DEST SPEC> :: <RF SPEC>↑<DM DEST>↑<PM SPEC>

<DM DEST> ::     DR1↑DR2↑DR3↑DR4↑DR5↑DR6↑
            DR7

<IAC> :: JZ↑POP↑PSH↑IAR↑IDR7↑SIRDY↑CB↑SF5↑SF6↑
         COF↑CIF↑SORDY↑SIPF↑SB↑SCC↑NOP↑CF5↑CF6↑
         SIRQ↑SDRQ↑CDEOR↑CDI1↑CDI2↑CDI3↑CDRQ↑
         CDIP↑SDF1↑SDF2↑SDF3↑SDFP↑0↑1↑
         2↑...↑IE↑IF

<ACT SPEC> :: <JUMP SPEC>↑<EMACT SPEC>↑
              <BRANCH SPEC>↑<GOTO SPEC>↑
              <NOP SPEC>

<BRANCH SPEC> :: BRANCH TO <EXP> <BTYPE>

<BTYPE> :: 4WAYS↑16WAYS↑256WAYS↑0↑1↑2↑...↑7

<JUMP SPEC> :: JUMP ON [NOT] <CONDITION> TO <EXP>

<GOTO SPEC> :: GOTO <EXP> ↑GO TO <EXP>

<CONDITION> :: T↑  SKSF↑OTAF↑INTF↑ARCO↑ORDY↑CCBT↑
               DR7CO↑      CCACO↑CCAHO↑DRQDP↑IRQ↑
               IRDY↑PIE↑CCAEZ↑EOR↑CCALEZ↑F5↑F6↑
               DIF1↑DIF2↑DIF3↑DIFP↑0↑1↑...↑IE↑IF

<EMACT SPEC> :: EMIT <EXP>↑ACT <EXP>↑
                ACT <EXP> EMIT <EXP>↑
                EMIT <EXP> ACT <EXP>

<NOP SPEC> :: NOP

<LABEL> :: ANY VALID SYMBOL ACCEPTABLE TO PMA.  THE
           DOLLAR SIGN ($) CHARACTER SHOULD NOT BE
           USED TO AVOID CONFLICT WITH INTERNAL
           SYMBOLS USED BY THE MACRO PACKAGE.
```



```
<EXP> :: ANY VALID PMA EXPRESSION.  LABELS ASSIGNED IN THE
         PROGRAM MAY BE USED, AS MAY ASTERISK (*), WHICH
         HAS ITS STANDARD VALUE (THE CURRENT PROGRAM
         COUNTER).  NOTE:  IF THE EXPRESSION CONTAINS ANY
         SPACES (AS ARE REQUIRED FOR PERIOD OPERATORS), THE
         ENTIRE EXPRESSION MUST BE SURROUNDED BY PARENTHESIS.
         EXPRESSIONS MUST NOT EXCEED 30 CHARACTERS IN LENGTH.
```

NOTES

1) IMPLICIT ALU MODE/FUNCTION SELECTION

THE FOLLOWING TABLE LISTS THE ALU MODE/FUNCTION SELECTIONS THAT ARE MADE FOR THE TRN, INC, DEC, NOT AND CON OPERATIONS:

OPERATION	ALU MODE/FUNCTION
TRN, BR SOURCE	$35
TRN, RF SOURCE	$30
INC	$10
DEC	$0F
NOT, BR SOURCE	$3A
NOT, RF SOURCE	$3F
CON, ZERO	$33
CON, MINUS1	$0C

2) <OP> ALU MODE/FUNCTION SELECT

<LOG OP> -- ALU MODE 3 (+ L) <ALUCS> MAY NOT BE SPECIFIED

- RF - $30
- AND - $31
- ZERO - $33
- OR - $34
- BR - $35
- XOR - $36
- BRN - $3A
- NOR - $3B
- ONE - $3C
- RFN - $3F

<AOP1> -- ALU MODE 0 (+ 0) <ALUCS> MAY BE SPECIFIED

PLUS - $06
LS - $03
SUB - $09

<AOP2> -- ALU MODE 1 (+ 1) <ALUCS> MAYNOT BE SPECIFIED

MINUS - $19

3) <RCM SPEC>

THE FORM 'RCM = <EXP>' IS USED TO BOTH SELECT THE BR SOURCE TO BE RCM AND TO SPECIFY AN EMIT FIELD CONSTANT (<EXP>). WHEN THIS FORM IS USED, THE <ACT SPEC> IN THE STATEMENT CAN ONLY BE NOP OR ACT <EXP>, AS ALL OTHERS CONFLICT WITH THE EMIT CONSTANT.

4) THE ASSEMBLY OF THE SOURCE FILE IS ACCOMPLISHED BY COPYING THE MPC MACRO INTO THE USERS UFD AND THEN SIMPLY STATING "PMA FILENAME". THE ASSEMBLER WILL CREATE THE BINARY AND LISTING FILES.

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8.0 FIELD ENGINEERING SWITCH PANEL

This panel consists (as far as the MPC's functionality with it is concerned) of three hexadecimal LED displays and three switches. The panel has a cable which plugs into the MPC back-edge connector F.

8.1 The three digit display shows the address of the next μ-program location to be accessed. The switches consist of a Single Cycle/Run switch, a Simulator/PROM switch, and Momentary Start switch.

8.2 The Single Cycle/Run switch, when in the Run position, causes the MPC clock to run continuously. In the Single Cycle position the MPC's clock will execute one cycle and then stop just prior to the end of clock 2 (see Figure 6-3). Thus the jump address, if any, will have been formed and be displayed, the register output will be valid and the output of the ALU will be valid. Depressing the Start switch will cause the MPC to execute the next cycle. When the switch is placed back in the Run position, the Start switch must be depressed if the program is to be continued from where it is or Master Clear must be activated or one of the two OCP Initializes must be issued if the program is to be started from location zero.

8.3 The Simulator/PROM switch determines the memory access timing. See Figure 6-2. When in the PROM position, the timing is set to run with PROM on the MPC board. When in the Simulator position, the third clock is doubled in length; thus adding one hundred nanoseconds to the memory access timing.

9.0 MPC OPERATION WITH A ROM SIMULATOR OR WRITABLE CONTROL STORE OR EXTERNAL ROM

The MPC may be connected to either the Signetics ROM Simulator or the PRIME Writable Control Store Option. This is done via four cables that plug into DIP sites on the MPC. When the μ-program being run is stored in either of these devices, the MPC must be placed in the simulator timing mode either via an OCP Simulator Initialize or the Simulator/PROM switch on the Field Engineering Switch Panel. This allows 100 ns longer for the memory access.

9.1 The Writable Control Store Option allows two modes of operation with the MPC. In the first mode, the MPC can execute μ-code out of the WCS PROM from addresses above 511 (currently up to 1023). This is known as the Extended Mode. It is done by simply addressing these locations. See Table 9-1.

In the second mode, the MPC may execute μ-code out of the writable memory on the WCS as though it were coming from any 256 word module; that is, from addresses 0 thru 255, or 256 thru 511, or 512 thru 767, or 768 thru 1023. See Table 9-1. This is done by issuing an OCP Stop to the MPC, loading the WCS RAM from main memory, OTA'ing configuration information to the WCS and then issuing an OCP Simulator Initialize to the MPC. The MPC will then execute the instruction starting in location zero.

USED ON	SCALE	SIZE	DWG. NO.	REV.
NEXT ASSY	SHEET 38 OF 40	A	SPC1409	1

Table 9-1

Writable Control Store
Memory Mapping

MPC u-Code Address	WCS Mode						
	Extended Mode	Extended Mode	Extended Mode	Simulate Mode	Simulate Mode	Simulate Mode	Simulate Mode
0 - 255	On Board PROM	On Board PROM	On Board PROM	RAM WCS	On Board PROM	On Board PROM	On Board PROM
256 - 511	On Board PROM	On Board PROM	On Board PROM	On Board PROM	RAM WCS	On Board PROM	On Board PROM
512 - 776	Slow PROM WCS	--	Slow PROM WCS	--	--	RAM WCS	--
777 - 1023	--	Slow PROM WCS	Slow PROM WCS	--	--	--	RAM WCS

9.2 To operate with the Signetics ROM Simulator, the four cables must be plugged into a junction box, which is then cabled to the MPC. Pins 14G-14 and/or 8N-15 must be grounded on the MPC. 14G-14 disables PROM outputs on the MPC of locations 0 thru 255 and 8N-15 disables PROM outputs from locations 256 thru 511. In addition, the MPC must be placed in the Simulator Timing Mode by either placing the switch on the Field Engineering Switch Panel (if connected) in the Simulator position or issuing an OCP Simulator Initialize. If it is desired to run with internal PROM with the ROM Simulator or external PROM still connected, one must ground pin 2L-14 to disable the external PROM.

9.3 To operate the MP with external ROM or PROM, a junction box must be used similar to that used with the ROM simulator to distribute addresses to the ROM/PROM chips and wire OR the output lines. Also the on board PROMs must be disabled by grounding the XTROM- and XTRIM- signals. Up to 1024 words of external PROM may be accessed. The cables to the external PROM must not exceed ten inches. These cables plug into the DIP sites shown in Table 9-2.

9.4 If one desires to run with external PROM or the ROM Simulator with the on board PROMs plugged in, one must ground pins 29K-1 and 33K-1 to disable the on board PROMs.

Table 9-2

MPC/ROM Sim/WCS Interface

DIP Site-Pin	Signal	DIP Site-Pin	Signal
2L-1	MCY09+	29M-1	RCC17+
2	MCY10+	2	RCC18+
3	MCY11+	3	RCC19+
4	MCY12+	4	RCC20+
5	MCY13+	5	RCC21+
6	MCY14+	6	RCC22+
7	MCY15+	7	RCC23+
8	GD04L+	8	RCC24+
9	MCY16+	9	RCC25+
10	MCY08+	10	RCC26+
11	MCY07+	11	RCC27+
12	XTROM-	12	RCC28+
13	XTR1M-	13	RCC29+
14	PULUP+G	14	RCC30+
15	GD04L+	15	RCC31+
16	PULUP+G	16	RCC32+
10L-1	RCC01+	45M-1	RCC33+
2	RCC02+	2	RCC34+
3	RCC03+	3	RCC35+
4	RCC04+	4	RCC36+
5	RCC05+	5	RCC37+
6	RCC06+	6	RCC38+
7	RCC07+	7	RCC39+
8	RCC08+	8	RCC40+
9	RCC09+	9	RCC41+
10	RCC10+	10	RCC42+
11	RCC11+	11	RCC43+
12	RCC12+	12	RCC44+
13	RCC13+	13	RCC45+
14	RCC14+	14	RCC46+
15	RCC15+	15	RCC47+
16	RCC16+	16	RCC48+

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A
PRWR
$(30)_{16}$ → DR0
ENABLE DMA CHAN
DAT REG(RB) → DR3
SELECT TO TRANSPORT
RF0 LS → RF0 C=1 PUSH
S4
START 5 SEC DELAY
S4
$(56)_{10}$ → RF8
RF0 LS → DR4 C=0 PUSH
LOL TO SELECTED TRANSPT
S4
LOL TRUE FOR 1 SEC
S4
$(56)_{10}$ → RF8
(60) → DR4 PUSH
LOL GOES FALSE
S4
1 SEC DELAY
S4
$(FD)_{16}$ → DR7
$(02)_{16}$ → DR4
LOL GOES TRUE
+1 → DR7
C.o DR7
N
Y
$(E4)_{16}$ → DR0
LOL GOES FALSE
(60) → DR4

BHOUSE
DAT REG(LB) → ALU SET CC (BIT 1)
BIT 1 = 1
Y
N
CTATJS ORDER?
ROUTINE TO PUT LATEST STATUS IN DAT REG
RF0 → DAT REG(LB)
$(23)_{16}$ ∧ RF4 → RF4
DR4 ∨ RF4 → RF4 → DAT REG(RB), SET FLG
DAT REG(LB) → ALU SET CC (BIT 3)
BIT 3 = 1
N
Y
CHANNEL NO. ORDER?
BCHANI
RF24 → DAT REG(LB) SET READY
(SHT 2)
M
DAT REG(LB) → ALU SET CC (BIT 4)
BIT 4 = 1
Y
N
VECTOR ADDRESS ORDER
RF31 → DAT REG(LB)
C
RF27 → DAT REG(RB) SET READY
FC REG → RF0
DAT REG(LB) → ALU SET CC (BIT 2)
BIT 2 = 1
N
Y
ID ORDER?
MODE REG → DR6
START SLOT NO. FORMTH
BIDI
$(0C)_{16}$ → DAT REG(RB)
RF0 ∧ $(C0)_{16}$ → RF0
DR6 RR → DR6
DR6(RR) ∨ RF0 → DR6
DR6 RR → DR6
DR6 RR → DR6
DR6 RR → DAT REG(LB) SET READY

C
START OF INT RTNE
BINTR
RF31 → ADDR(LB) SET INT REQ
RF27 → ADDR(RB) RESET BUSY
BEGIN
(00) → DR2 CLEAR DIL p
OTA FLAG SET
N
Y
FROM INIT RTNE
E
BMOT
DAT REG(RB) → RF1
SELECT TO DRIVES
$(0F)_{16}$ ∧ RF1 → DR3
DAT REG(LB) → RF29 SET CC (BIT 1)
SELECT ONLY ORDER?
BIT 1 = 1
N
B
RF21 + SKS(LB) + 1 → SKS(LB)
SET SKS "INCORRECT"
Y
DRR → RF30

D
BCYCLE
SELECT TRANS #0
(08) → RF0, DR3
(80) → RF1 SET DIL #2
OTA FLAG SET
N
Y
BSID
OTA FC REG → RF1 SET μ BUSY
RF1 ∧ (0F) → RF1 CLEAR OTA FLAG
RF1 − (01) → ALU SET CC (ZERO)
(00) → DR4
ZERO
OTA MOTION SET UP?
Y
N
RF1 − $(00)_{16}$ → ALU SET CC − (ZERO)
ZERO
N
Y
BCHAN
DAT REG(LB) → RF24
DAT REG(RB) → RF25
BMRDY
(80) → RF8, SKS(LB) CLEAR μ BUSY
DIL #2 SET
N
Y
TRANS DLY LOOP OVER?
F
D
OTA VECTOR ADDRESS INSTR COMPLETE
RF1 − $(0E)_{16}$ → ALU SET CC − (ZERO)
ZERO
OTA INT VECTOR?
N
Y
BVECT
DAT REG(LB) → RF31
DAT REG(RB) → RF27
RESELECT TRANS
RF30 ∧ $(0F)_{16}$ → DR3
RF1 − (02) → ALU SET CC (ZERO)
ZERO
OTA HOUSE-KEEPING SETUP?
Y
RF21 + SKS(LB) + 1 → SKS(LB)
N
RF1 − (03) → ALU SET CC (ZERO)
(60) → RF0
A
ZERO
OTA PWR ON?
Y
N
C

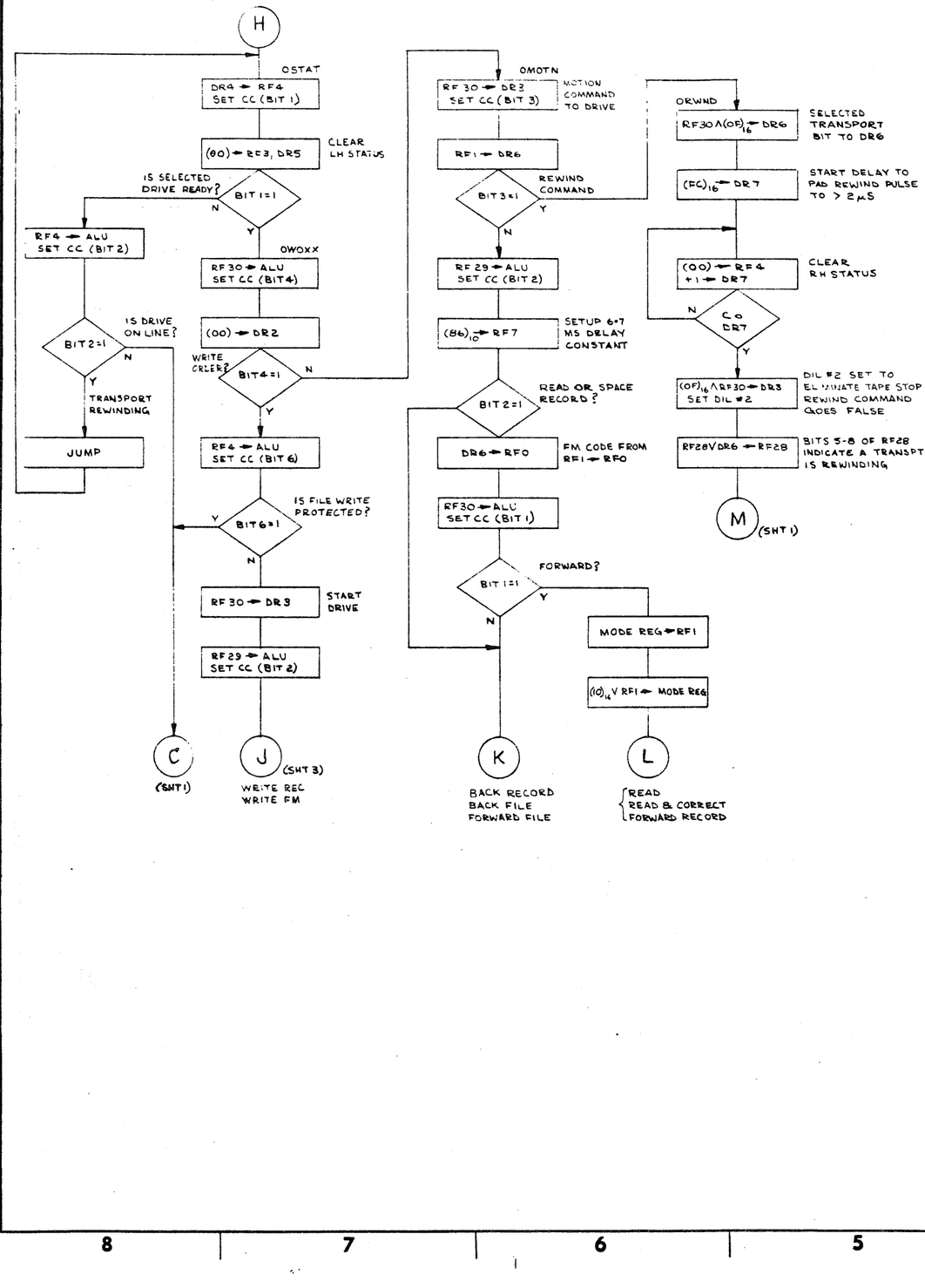
BTRWD3
RF1 − 1 → RF1 SET CC − (BIT 1)
ROUTINE TO RESTORE RF28 TO ORIGINAL POSITION
BIT 1 = 1
Y
IF RF28 IN ORIGINAL POSITION?
RF28 → DR6
N
BTRWD2
DR6 RR → RF28, DR6
START OF ROUTINE TO TEST IF REWINDING TRANSPORTS HAVE FINISHED
BTRWD1
RF28 → ALU SET CC (BIT 5)
RF0 → DR6
BIT 5 = 1
N
Y
TRANSPT GIVEN REWIND ORDER?
DR4 → ALU SET CC (BIT 4)
IS TRANSPT STILL RE-WINDING?
BIT 4 = 1
N
RF0 → DR7
Y
OTA FLAG SET
Y
DR6 RR → RF0
N
SELECT NEXT TRANSPORT
RF0 ∧ $(0F)_{16}$ → RF0, DR3
RF28 LS → RF28 C=0
RF1 + 1 → RF1 SET CC (BIT 6)
ALL 4 TRANSPTS TESTED?
BIT 6 = 1
N
Y
BRWDF
RF1 − 1 → RF1 SET CC − (BIT 1)
RF28 → DR6, SET BUSY
BIT 1 = 1
Y
N
DR6 RR → RF28, DR6
SET REWIND INT. STATUS AND SKS INCORRECT
BSRWIS
$(01)_{16}$ ∨ RF4 → RF4, SKS(LB)
RF28 ⊕ DR7 → RF28
CLEAR REWIND BIT
E
OTA FLAG SET
Y
N
JUMP

G
(SHT 4)
BEGIN
RF2 → ADDR (RB) CLEAR DIL #2
LOAD INTERR VECTOR
$(107)_{10}$ → RF7 SET INT R2Q
TO GIVE 8·3 MS DLY
RF31 → ADDR (LB) RESET BUSY
LOAD INTERR VECTOR
F
BTSD
RF8 + 1 → RF8 PUSH
GO TO TAPE STOP DLY SUB
S4
S4
WAS OTA FLAG SET
OTA FLAG SET
Y
E
N
JUMP
D

PRELIMINARY ISSUE
APPRD FOR PROTOTYPE
DATE

II-1

MATERIAL	DWN Paul Fontaine	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK	MAGNETIC TAPE CONTROLLER (NRZ) BEGINNING AND ENDING	
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES: –DIMENSIONS ARE IN INCHES –TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.		
	APPRD		
USED ON	SCALE	SIZE D	DWG. NO. MIC1657 REV. 2
NEXT ASSY	SHEET 1 OF 6		



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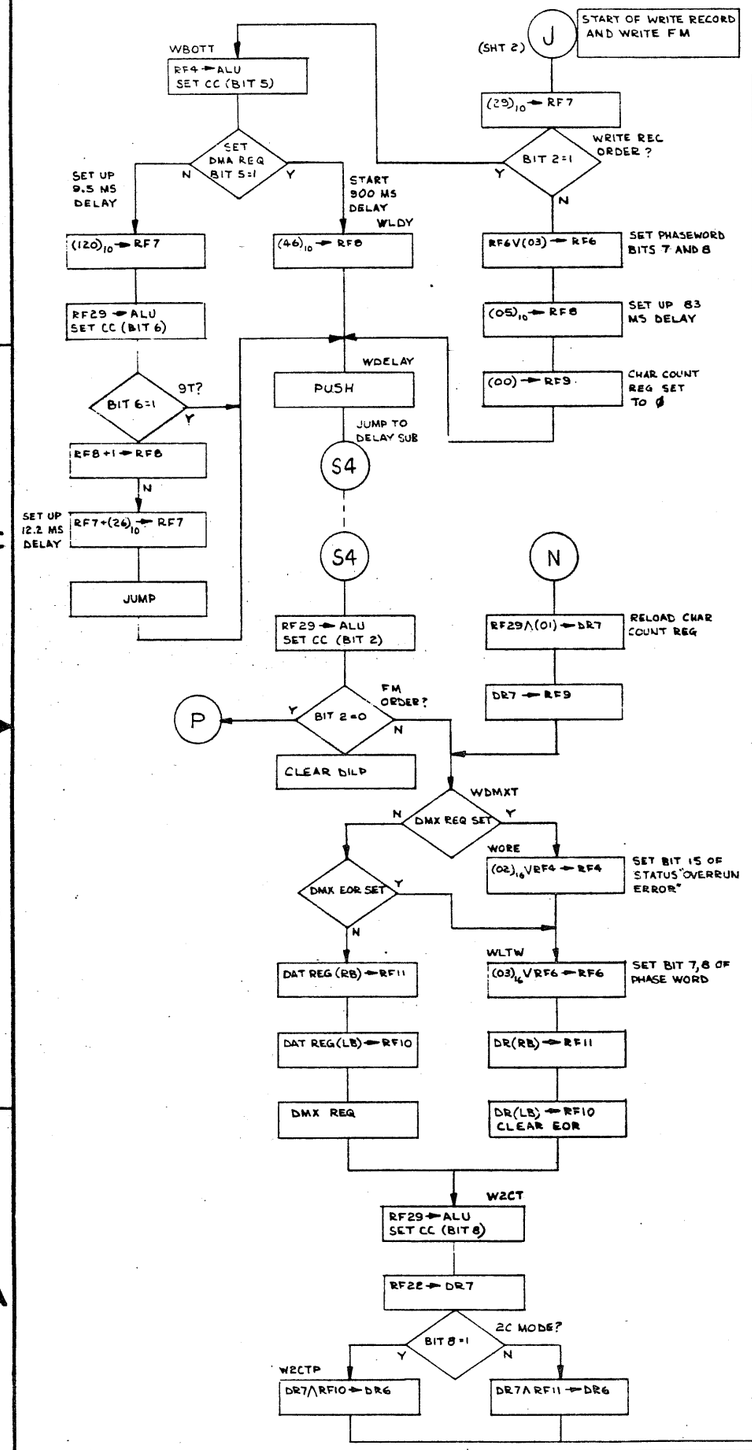
PRELIMINARY ISSUE

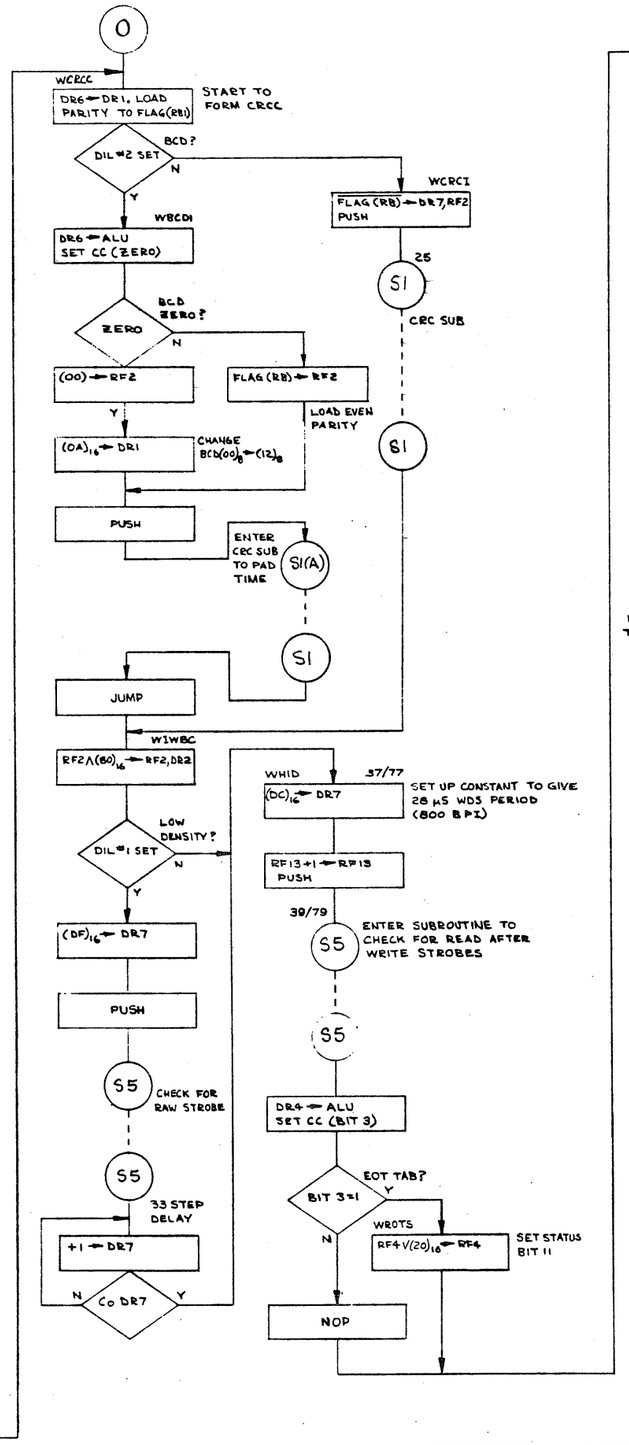
APPRD FOR PROTOTYPE _____ DATE _____

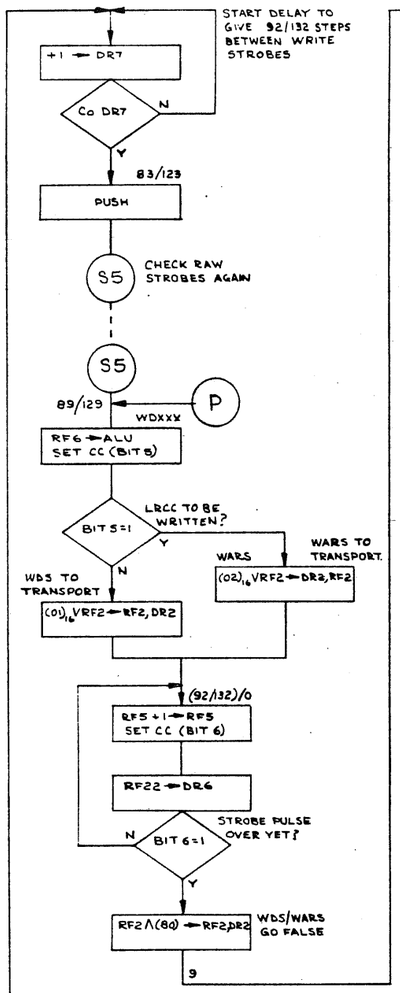
II-2

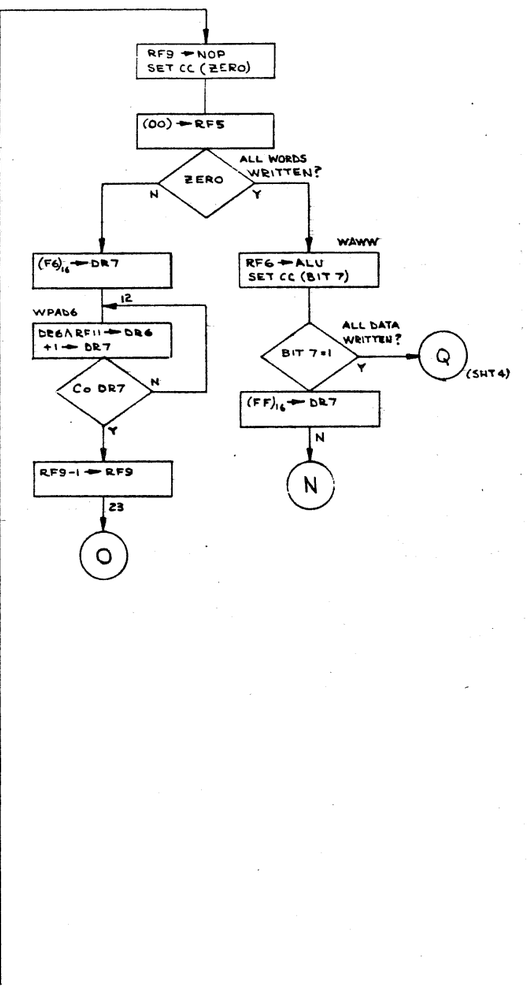
MATERIAL	DWN 6-2-76 Jack Evans	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES: –DIMENSIONS ARE IN INCHES –TOLERANCES XX ± .02, XXX ± .005, ANGLES ± 1/2°	ENG.	MAGNETIC TAPE CONTROLLER (NRZ) ORDER DECODE
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 7 OF 23 / SIZE D / DWG. NO. MIC 1657 / REV. 3

LTR	DATE	REVISION	DR.	CK.





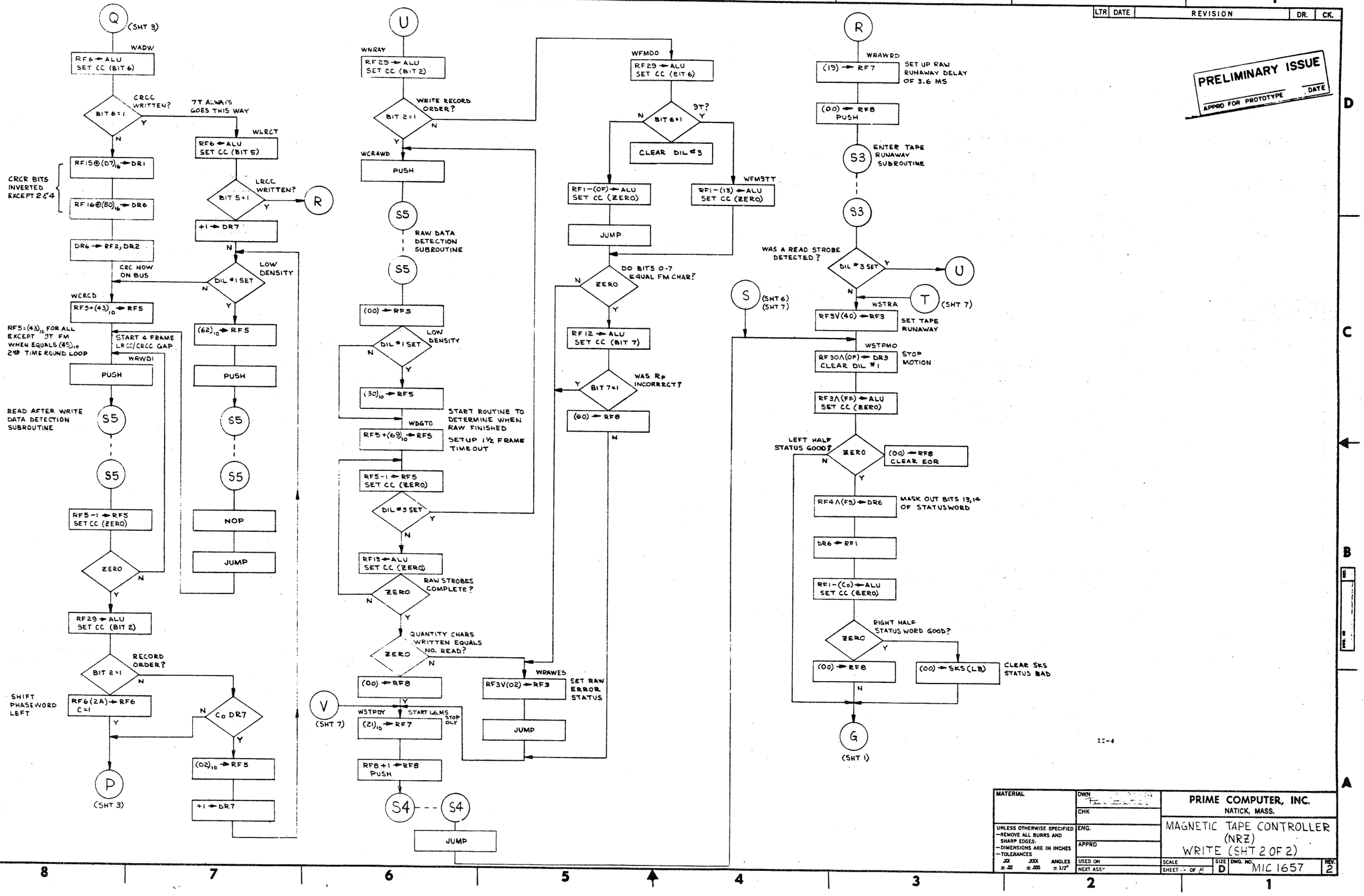




PRELIMINARY ISSUE

APPRD FOR PROTOTYPE ____ DATE ____

MATERIAL	DWN 5-05-74 Paul Bate	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES: –DIMENSIONS ARE IN INCHES –TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK ENG. APPRD USED ON NEXT ASSY	MAGNETIC TAPE CONTROLLER (NRZ) WRITE (SHT 1 OF 2)
	SCALE SHEET 1 OF 8	SIZE D DWG. NO. MIC 1657 REV. 3


Q
(SHT 3)
WADW
RF6 → ALU
SET CC (BIT 6)
CRCC WRITTEN?
BIT 6=1
Y
N
7T ALWAYS GOES THIS WAY
WLRCT
RF6 → ALU
SET CC (BIT 5)
LRCC WRITTEN?
BIT 5=1
Y
R
CRCR BITS INVERTED EXCEPT 2,5,4
RF15⊕(D7)16 → DR1
RF16⊕(80)16 → DR6
+1 → DR7
N
DR6 → RF2, DR2
CRC NOW ON BUS
LOW DENSITY
DIL #1 SET
N
Y
WCRCD
RF5+(43)10 → RF5
(62)10 → RF5
RF5=(43)10 FOR ALL EXCEPT 9T FM WHEN EQUALS (45)10 2ND TIME ROUND LOOP
START 4 FRAME LRCC/CRCC GAP
WRWDI
PUSH
PUSH
READ AFTER WRITE DATA DETECTION SUBROUTINE
S5
S5
S5
S5
RF5-1 → RF5
SET CC (ZERO)
NOP
ZERO
N
JUMP
Y
RF29 → ALU
SET CC (BIT 2)
BIT 2=1
RECORD ORDER?
N
SHIFT PHASEWORD LEFT
RF6(2A) → RF6
C=1
Y
N
Co DR7
Y
(02)10 → RF5
+1 → DR7
P
(SHT 3)
U
WNRAW
RF29 → ALU
SET CC (BIT 2)
WRITE RECORD ORDER?
BIT 2=1
N
Y
WCRAWD
PUSH
S5
RAW DATA DETECTION SUBROUTINE
S5
(00) → RF5
LOW DENSITY
DIL #1 SET
N
Y
(30)10 → RF5
START ROUTINE TO DETERMINE WHEN RAW FINISHED
WDGTO
RF5+(69)10 → RF5
SETUP 1½ FRAME TIME OUT
RF5-1 → RF5
SET CC (ZERO)
DIL #3 SET
Y
N
RF13 → ALU
SET CC (ZERO)
ZERO
RAW STROBES COMPLETE?
N
Y
QUANTITY CHARS WRITTEN EQUALS NO. READ?
ZERO
N
WRAWES
RF3V(02) → RF3
SET RAW ERROR STATUS
(00) → RF8
Y
V
(SHT 7)
WSTPDY
START 1.6MS STOP DLY
(21)10 → RF7
JUMP
RF8+1 → RF8
PUSH
S4
S4
JUMP
WFMDO
RF29 → ALU
SET CC (BIT 6)
9T?
BIT 6=1
N
Y
CLEAR DIL #3
RF1-(0F) → ALU
SET CC (ZERO)
WFM9TT
RF1-(13) → ALU
SET CC (ZERO)
JUMP
DO BITS 0-7 EQUAL FM CHAR?
ZERO
N
Y
RF12 → ALU
SET CC (BIT 7)
WAS Rp INCORRECT?
BIT 7=1
Y
(60) → RF8
N
R
WRAWRD
(19) → RF7
SET UP RAW RUNAWAY DELAY OF 3.6 MS
(00) → RF8
PUSH
S3
ENTER TAPE RUNAWAY SUBROUTINE
S3
WAS A READ STROBE DETECTED?
DIL #3 SET
Y
U
N
WSTRA
T
(SHT 7)
S
(SHT 6)
(SHT 7)
RF3V(40) → RF3
SET TAPE RUNAWAY
WSTPMO
RF30Λ(0F) → DR3
CLEAR DIL #1
STOP MOTION
RF3Λ(FF) → ALU
SET CC (ZERO)
LEFT HALF STATUS GOOD?
ZERO
N
(00) → RF8
CLEAR EOR
Y
RF4Λ(F3) → DR6
MASK OUT BITS 13,14 OF STATUSWORD
DR6 → RF1
RF1-(Co) → ALU
SET CC (ZERO)
RIGHT HALF STATUS WORD GOOD?
ZERO
Y
(00) → RF8
(00) → SKS(LB)
CLEAR SKS STATUS BAD
N
G
(SHT 1)
LTR
DATE
REVISION
DR.
CK.
PRELIMINARY ISSUE
APPRD FOR PROTOTYPE
DATE
II-4
MATERIAL
DWN
CHK
ENG.
APPRD
USED ON
NEXT ASSY
UNLESS OTHERWISE SPECIFIED
—REMOVE ALL BURRS AND SHARP EDGES:
—DIMENSIONS ARE IN INCHES
—TOLERANCES
.XX ±.02
.XXX ±.005
ANGLES ±1/2°
PRIME COMPUTER, INC.
NATICK, MASS.
MAGNETIC TAPE CONTROLLER (NRZ)
WRITE (SHT 2 OF 2)
SCALE
SHEET - OF 2
SIZE D
DWG. NO. MIC 1657
REV. 2

LTR	DATE	REVISION	DR.	CK.

START OF READ RECORD
FORWARD RECORD
READ & CORRECT

(L) (SHT 2)

RF4 → ALU
SET CC (BIT 5)

LOADPOINT?
BIT 5 = 1
N
Y

START 6.7 MS DELAY

$(01)_{10}$ → RF8
SET UP 26 MS DELAY

RSDLY
RF8 + 1 → RF8
PUSH

GO TO DELAY SUBROUTINE

(S4)

(S4)

SET UP 500 MS RUNAWAY DELAY

$(26)_0$ → RF8
CLEAR DILP

PUSH

TAPE RUNAWAY SUBROUTINE

(S3)

(S3)

READ STB REC'D?
DIL #3 SET
Y

(00) → RF22

N

(T) (SHT 4)

(W)

RDAT
CLEAR DIL #3

DIL #2 SET
BCD?
N
Y

(Y)

RBCDM
PARITY FLAG=0
PARITY OKAY?
Y
N

JUMP

(X)

PARITY OKAY?
PARITY FLAG=1
RBINM
Y
N

RTCOR
RF29 → ALU
SET CC (BIT 4)

READ & CORRECT
BIT 4 = 1
Y
N

INVERT DATA BIT CORRESPONDING TO ERROR TRACK
DR6 ⊕ RF26 → DR6

RF23 ⊕ DR7 → DR7

SET BIT 1 OF STATUS
RVPET
$(80)_{16}$ V RF3 → RF3

RFMVER
RF0 - DR6 → ALU

RF22+1 → RF22

DATA READ (0→7) EQUAL FM?
ZERO
N
Y

DR7 → ALU
SET CC (BIT 7)

NOT A COMPLETE FM?
Y
BIT 7 = 1
N

RF13 + 1 → RF13
RF13 COUNTS FM'S READ

RLRCUP
DR6 ⊕ RF19 → RF19
UPDATE LRC

DR7 ⊕ RF20 → RF20
UPDATE LRC

BCD?
DIL #2 SET
N
Y

RF1 - (0A) → ALU
SET CC (ZERO)

BCD I/P CHAR $(12)_8$?
ZERO
N
Y

(00) → RF1, DR6

REOTD
DR4 → ALU
SET CC (BIT 3)

EOT TAB?
BIT 3 = 1
N

DR7 → RF12
READ PARITY (CORRECTED) IS IN DR7

Y

RF4 V (20) → RF4
SET EOT STATUS BIT

RTFRI
RF29 → ALU
SET CC (BIT 3)

DR6 → RF1
READ DATA (CORRECTED) IS IN DR6

FORWARD RECORD?
BIT 3 = 1
N
Y

(Z)

REPRR
UPDATE EPR ROUTINE
RF17 → DR6

DR6 RR → RF17, DR6

DR6 → RF14

RF14 = TEMP STORAGE

RF17 Λ $(7F)_{16}$ → RF17, DR7

DR7 V RF18 → DR7

DR7 → RF17
EPR III RF17 HAS BEEN ROTATED 1 RIGHT

PARITY CORRECT?
PARITY FLAG=1
Y
N

RF 4 Λ $(80)_6$ → DR7
SET CC (BIT 1)

JUMP

REPPI
RF14 Λ $(80)_{16}$ → DR7
SET CC (BIT 1)

INVERT EP & MASK OUT UNWANTED BITS

CLEAR DILP

Ep=0
Ep=1?
N
DR7 → RF18 BIT 1 = 1
Y

RF17 ⊕ $(3C)_{16}$ → RF17
INVERT E_{2-5} IF Ep=1

EPR HAS BEEN UPDATED
MOVE READ PARITY BIT TO BIT 1 OF DR7

RF12 → ALU
SET CC (BIT 7)

(00) → DR7, RF12

BIT 7 = 1
N
Y

(80) → DR7, RF12

RF1 → DR6
PUSH

(S1) GO TO CRC SUBROUTINE

(S1)

RECRCR
RF6 → ALU
SET CC (BIT 4)

(00) → RF5

READ CRCC PHASE?
BIT 4 = 1
Y
N

(AA) (SHT 6)

LOW DENSITY?
DIL #1 SET
N
Y

$(50)_{10}$ → RF5

RF5 + $(113)_{10}$ → RF5

RF5 SET TO GIVE 2½ FRAME GAP

(00) → RF7
PUSH

EXIT TO DETECT READ STROBE DURING DELAY SUB

(S3)

(S3)

DIL #3 SET
Y

(W)

(00) → RF7

N

(00) → RF5

LOW DENSITY?
DIL #1 SET
N
Y

$(60)_{10}$ → RF5

RF5 + $(136)_{10}$ → RF5
SET UP RF5 FOR 3 FRAME GAP

(00) → DR7
PUSH

EXIT TO DETECT READ STROBE DURING DELAY

(S3)
1 CRC(9T)
1 OR LRC(7T)
1 EXPECTED

(S3)

RF20 → ALU
SET CC (BIT 8)

RF9 → ALU
SET CC (ZERO)

2C?
BIT 8 = 1
N
Y

DATA TRANSFER LEFT?
ZERO
N
Y

(00) → DR (RB)

DMX REQ SET
N
Y

RDORS2
RF4 V (02) → RF4
SET DMX OVERRUN STATUS

RF10 → DR (LB)

SET DMX REQ

RDTTI
RF 29 → ALU
SET CC (BIT 6)

RF9+1 → RF9
FOR 9T TO ENSURE NO MORE DATA TRANSFERS

9T
BIT 6 = 1
N
Y

(BB) (SHT 6)

WAS THERE A CRC?
DIL #3 SET
Y
N

RF6 V $(01)_{16}$ → RF6
SET DIFP
FORCE PARITY SET AND FORCE ODD NO. CHARS.

RF6 ⊕ $(10)_{16}$ → RF6
SET CC BIT 8

RF22-1 → RF22
CLEAR DIL #3

ODD NO CHARS READ?
BIT 8 = 1
Y
N

JUMP

(X)

(Y)

PRELIMINARY ISSUE
APPRD FOR PROTOTYPE — DATE

RF9 → ALU
SET CC (ZERO)

RF6 ⊕ (01) → RF6
INVERT BIT 8 OF RF6 TO COUNT ODD/EVEN

DEC RF9 → RF9

ALL WORD READ?
ZERO
Y
N

RAWR
DR6 → RF11

REQDMX
DMX REQ SET
Y

RDORS1
SET BIT IS IN STATUSWORD
$(02)_{16}$ V RF4 → RF4

(Z)

RF10 → DR (LB)
N

(CC) (SHT 6)

DR6 → RF10

(Z)

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES: .XX ± .02, .XXX ± .005, ANGLES ± 1/2°	ENG.	MAGNETIC TAPE CONTROLLER (NRZ) READ (SHT 1 OF 2)
	APPRD	
USED ON	SCALE	SIZE D — DWG. NO. MIC1657 — REV. 2
NEXT ASSY	SHEET 5 OF 7	

II-5

LTR	DATE	REVISION	DR.	CK.

AA (SHT 5)

RCRCTR

RF16 → ALU SET CC (BIT 1) — START CRCR= MATCH PATTERN

RF15 → DR6

BIT 1 = 1? (N / Y)

RF15 ⊕ $(28)_{16}$ → RF15 — INVERT BITS 2 & 4

RF15+1 → ALU SET CC (ZERO)

DR6 → RF15

ZERO? (N / Y) — CRCC OKAY?

RCRCER

$(20)_{16}$ V RF3 → RF3 — SET BIT 3 OF STATUS

RLRCCD

$(D6)_{16}$ → RF5 — LOOK FOR LRCC

RF5 SET TO GIVE 5 FRAME GAP

$(6C)_{16}$ → RF7 PUSH

S3 — DETECT LRCC SUBROUTINE

S3

WAS LRCC FOUND? DIL #3 SET? (Y / N)

BB (SHT 5)

RLRCCK

RF19 ⊕ DR6 → RF19 SET CC (ZERO)

CLEAR DIL #3

LRCp=7 TEST OKAY? ZERO? (N / Y)

DR7 ⊕ RF20 → RF20 SET CC (BIT 7)

LRCp TESTS BAD? BIT 7 = 1? (Y / N)

RLRCER

RF3 V (10) → RF3 — SET BIT 4 STATUS

JUMP

REORGD

SET UP RF5 & RF7 TO GIVE 16 FRAME GAP

$(5C)_{16}$ → RF5

(00) → RF7

LOW DENSITY — DIL #1 SET? (N / Y)

(02) → RF7

RF7+(03) → RF7 CLEAR DIL #3

RFGDY

EFS → EFS SET CC (ZERO) DIL #3 SET? (Y / N) — FALSE GAP PREVIOUSLY DETECTED

EFSD

$(08)_{16}$ V RF3 → RF3 CLEAR DIL #3 — SET BIT 5 OF STATUS

ZERO? (N / Y)

JUMP

GAP WILL BE SHORTER IF FALSE DATA FOUND

RFGDY1

RF7-1 → RF7 SET CC (ZERO) DIL #3 SET? (Y / N)

16 FRAME GAP OVER? ZERO? (N / Y)

(0F) ∧ RF30 → DR3 CLEAR DIL #1

DD

DD

RF13-1 → RF13 SET CC (ZERO)

RF22-1 → RF22 SET CC (ZERO)

ZERO? (N / Y) — ONLY ONE FM CHAR READ?

ZERO? (N / Y) — ONLY ONE CHAR READ

RF3 → ALU SET CC (BIT 4)

LRC BAD? BIT 4 = 1? (Y / N)

RFIN

RF29 → ALU SET CC (BIT 3)

(00) → RF23

BIT 3 = 1? (Y / N) — FORWARD RECORD?

RF29 → ALU SET CC (BIT 6)

9T? BIT 6 = 1? (N / Y)

(00) → RF26

RF3 → ALU SET CC (BIT 3)

TEST CRC ERROR FLAG TO DETERMINE IF TRACK IDENT IS REQUIRED

BIT 3 = 1? (N / Y)

RF26+1 → RF26 — SET BIT 8 OF TER TO INITIAL STATE

RTIER1

$(D7)_{16}$ ⊕ RF15 → DR6 — INVERT CRCR BITS EXCEPT 2 & 4

$(80)_{16}$ ⊕ RF16 → DR7

DR7 ⊕ RF18 → ALU SET CC (BIT 1) — COMPARE PARITY BITS OF EPR & CRCR

CRCRp = EPRp? BIT 1 = 0? (N / Y)

RF17 - DR6 → ALU SET CC (ZERO) — COMPARE CRCR (0-7) WITH EPR (0-7)

$CRCR_{0\to7} \equiv EPR_{0\to7}$? ZERO? (N / Y)

RF23 → RF23 C=0 — THIS SETS BIT 7 OF TER (P) IF RF23 WAS SET PREVIOUSLY

S (SHT 4)

RF3+1 → RF3 — SET FM STATUS BIT 8

RFRC2

RF3 ∧ (49) → RF3 — CLEAN UP STATUS BITS

JUMP

RTIER2

RF23 → ALU SET CC (BIT 8)

ERROR UNCORRECTABLE — BIT 8 = 1? (Y / N) — (00) → DR7

RUCED

$(04)_{16}$ V RF3 → RF3 — SET BIT 6 OF STATUS

JUMP

START CRC UPDATE

$(00)_{16}$ → DR6 PUSH

S1

SHIFT CRCR SUB

S1

RTIER3

SHIFT TER TO DENOTE NEXT TRACK

RF26 2A → RF26 SET CC C=0

8 COMPARES FAILED? ZERO? (Y / N)

RF23+1 → RF23

CC (SHT 5)

RF11 → DAT REG (RB)

EOR SET? (N / Y)

RNEORS

SET DMX

RF3 V (08) → RF3 — SET INADEQUATE RANGE STATUS BIT

RRCCR

RF29 ∧ (01) → DR7

DR7 → RF9

Z (SHT 5)

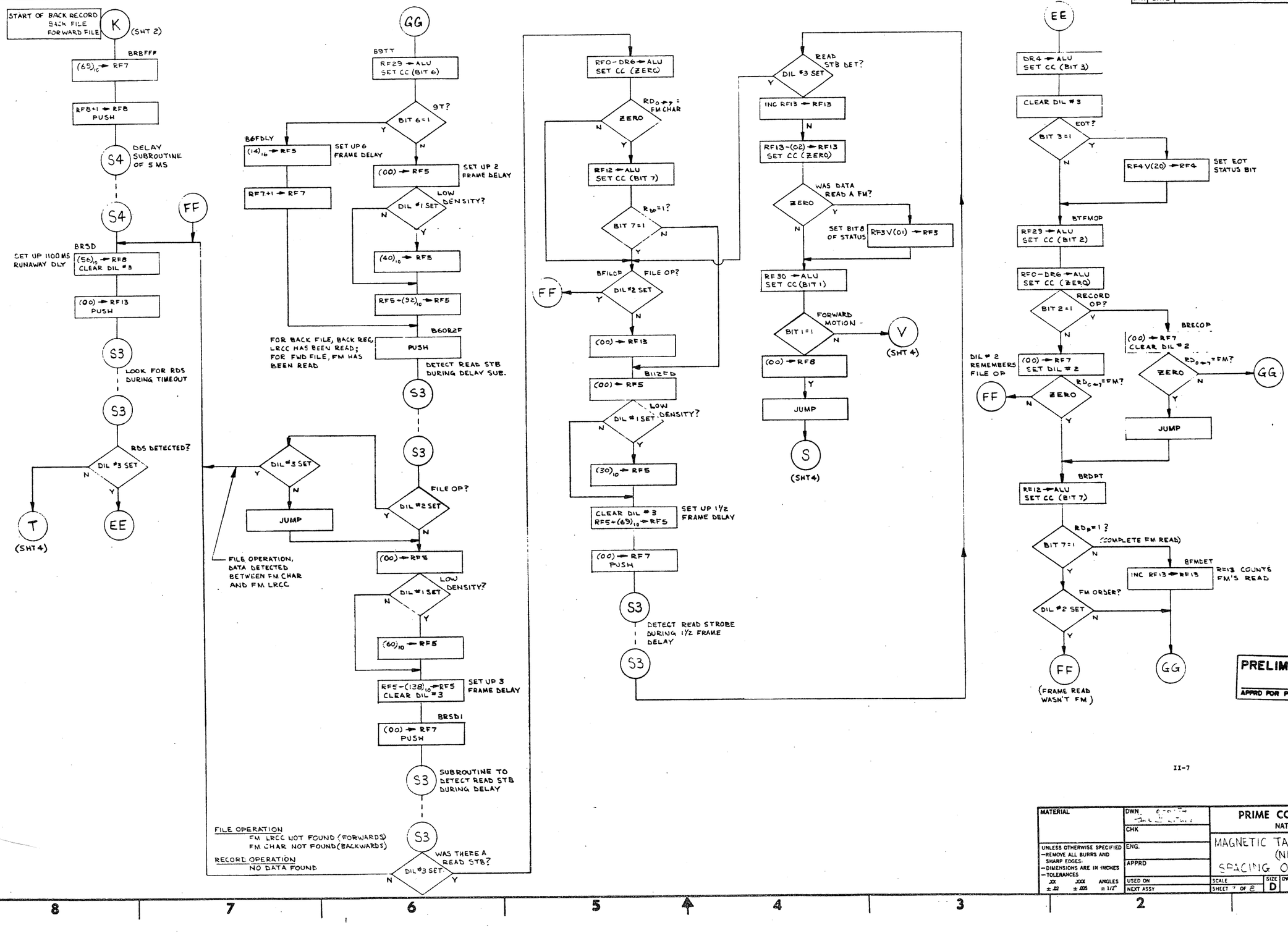
PRELIMINARY ISSUE

APPRD FOR PROTOTYPE ____ DATE

II-6

MATERIAL	DWN Paul Bastone	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES. —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	MAGNETIC TAPE CONTROLLER (NRZ) READ (SHT 2 OF 2)	
	APPRD		
	USED ON	SCALE	SIZE D DWG. NO. MIC 1657 REV. 2
	NEXT ASSY	SHEET 5 OF 5	

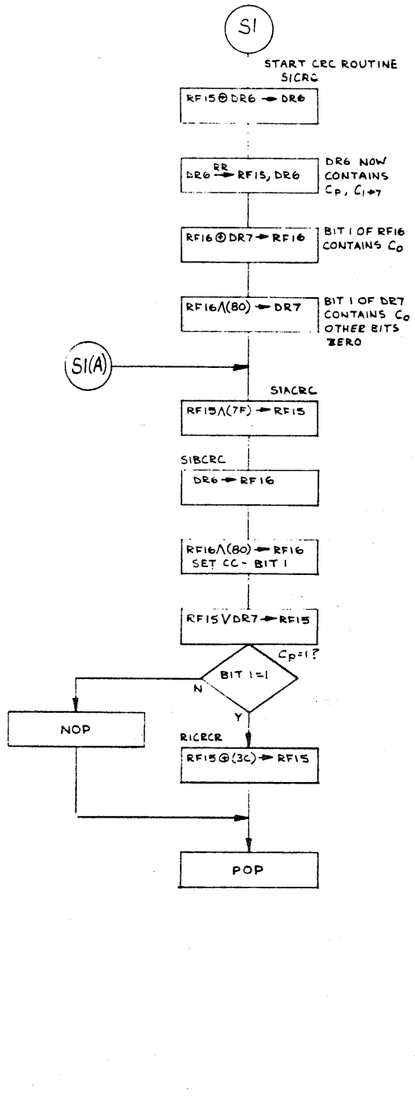
LTR	DATE	REVISION	DR.	CK.

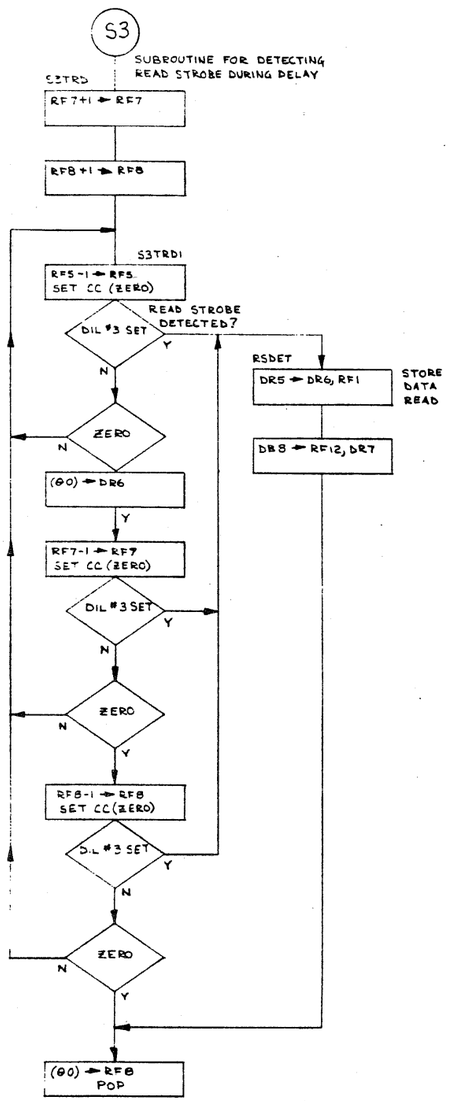


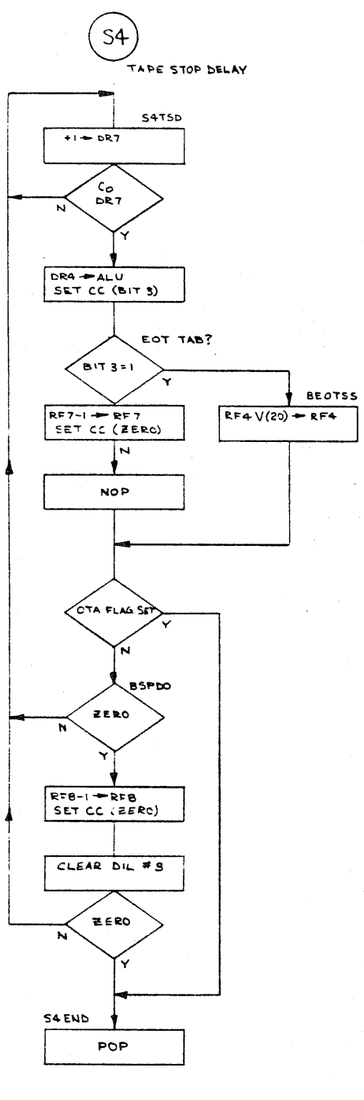
PRELIMINARY ISSUE

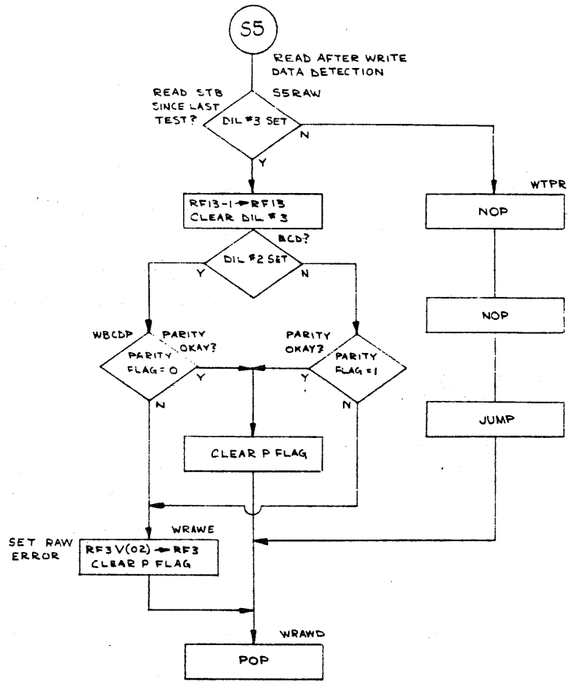
APPRD FOR PROTOTYPE _____ DATE

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES: –DIMENSIONS ARE IN INCHES –TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	MAGNETIC TAPE CONTROLLER (NRZ) SPACING OPERATIONS
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 7 OF 8 / SIZE D / DWG. NO. MIC1657 / REV. 2









LTR	DATE	REVISION	DR.	CK.

PRELIMINARY ISSUE
APPRD FOR PROTOTYPE ____ DATE

MATERIAL	DWN Frank E.	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	MAGNETIC TAPE CONTROLLER (NRZ) SUBROUTINES
	APPRD	
USED ON	NEXT ASSY	SCALE — SHEET 7 OF 15 · SIZE D · DWG. NO. MIC1657 · REV. 2

```
                    (0001) *     FILE MTNRZ9   NOV 11 1974   REV 9
                    (0002) *
                    (0003) *
                    (0004) *      MAG TAPE CONTROLLER
                    (0005) *
                    (0006) *
                    (0007) *
                    (0008) *              *************
                    (0009) *              *           *
                    (0010) *              * P R 1 M E *
                    (0011) *              *           *
                    (0012) *              *   M P C   *
                    (0013) *              *           *
                    (0014) *              * ASSEMBLER *
                    (0015) *              *           *
                    (0016) *              *************
                    (0017) *
                    (0018) *
                    (0019) *
                    (0936) *
                    (0937) *
                    (0938) *
                    (0939) * INITIALIZE ROUTINE AT MICRO-CODE LOCATION ZERO
                    (0940) *
                    (0941) INIT   MPC     CON ZERO => (DR7, OFC) SB
000: 0006 F9B8 0000
                    (0942)        MPC     CON ZERO => RFDR7 ;
                    (0943)                IDR7      JUMP ON NOT DR7C0 TO *
001: 0201 1990 4001
                    (0944)        MPC     TRN RCM => DR0 ;
                    (0945)                COF       EMIT $E4
002: 0002 1A9D 00E4
                    (0946)        MPC     CON ZERO => (DR3, MR)  SDF2
003: 0006 79E4 0000
                    (0947)        MPC     CON ZERO => (DR6, SRL) CDEOR
004: 0006 D9CC 0000
                    (0948) *
                    (0949) *   8.3 MS TAPE STOP DELAY
```



```
                    (0950) *
                    (0951)        MPC     TRN RCM => RF 7 ;
                    (0952)                CIF       EMIT 107
005: 0039 1AA1 006B
                    (0953)        MPC     INC RF 8 => RF 8 ;
                    (0954)                PSH       GOTO S4TSD
006: 0041 0808 802E
                    (0955) *
                    (0956) * LOAD STANDARD VECTOR ADDRESS
                    (0957) *
                    (0958)        MPC     TRN RCM => RF 27 ;
                    (0959)                CB        EMIT $4C
007: 00D9 1A99 004C
                    (0960) *
                    (0961) * ENTRY POINT FROM INITIALIZE ROUTINE AND INTERRUPT REQUEST
                    (0962) *
                    (0963) BEGIN  MPC     CON ZERO => DR2 ;
                    (0964)                CDIP       JUMP ON NOT OTAF TO *
008: 0002 59DC 0C08
                    (0965) BSID   MPC     TRN  OFC => RF 1 ;
                    (0966)                SB
009: 5C09 1AB8 0000
                    (0967)        MPC     RF 1 AND RCM => RF 1 ;
                    (0968)                COF       EMIT $0F
00A: 0009 189D 000F
                    (0969)        MPC     DEC RF 1 => NOP ;
                    (0970)                SCC
00B: 0008 07BC 0000
                    (0971)        MPC     CON ZERO => DR4   NOP   JUMP ON CCAEZ TO BMOT
00C: 0002 99C0 E44A
                    (0972)        MPC     RF 1 MINUS RCM => NOP ;
                    (0973)                SCC       EMIT $0C
00D: 0008 0CBD 000C
                    (0974)        MPC     CON ZERO => NOP ;
                    (0975)                NOP       JUMP ON CCAEZ TO BCHAN
00E: 0000 19C0 E442
                    (0976)        MPC     RF 1 MINUS RCM => NOP ;
                    (0977)                SCC       EMIT $0E
```



```
00F: 0008 0CBD 000E
                    (0978)        MPC     CON ZERO => NOP ;
                    (0979)                NOP       JUMP ON CCAEZ TO BVECT
010: 0000 19C0 E448
                    (0980)        MPC     RF 30 AND RCM => DR3 ;
                    (0981)                NOP       EMIT $0F
011: 00F2 78C1 000F
                    (0982)        MPC     RF 1 MINUS RCM => NOP ;
                    (0983)                SCC       EMIT $02
012: 0008 0CBD 0002
                    (0984)        MPC     RF 21 PLUS SRL + 1 => SRL ;
                    (0985)                NOP       JUMP ON CCAEZ TO BHOUSE
013: 58AC CB40 E5C8
                    (0986)        MPC     RF 1 MINUS RCM => NOP ;
                    (0987)                SCC       EMIT $03
014: 0008 0CBD 0003
                    (0988)        MPC     CON ZERO => RF 0 ;
                    (0989)                NOP       JUMP ON CCAEZ TO BPWR
015: 0001 19C0 E5BC
                    (0990) BINTR  MPC     TRN RF 31 =>  ARL SIRQ
016: 00FC B844 0000
                    (0991)        MPC     TRN RF 27 =>  ARR ;
                    (0992)                CB      GOTO BEGIN
017: 00DC 3818 8008
                    (0993) *
                    (0994) *
                    (0995) * SUBROUTINE, CRC
                    (0996) *
                    (0997) S1CRC  MPC     RF 15 XOR DR6 => DR6
018: 347A D840 0000
                    (0998)        MPC     TRN DR6RR => (RF 15,DR6)
019: 947B DAC0 0000
                    (0999)        MPC     RF 16 XOR DR7 => RF 16
01A: A081 1840 0000
                    (1000)        MPC     RF 16 AND RCM => DR7 ;
                    (1001)                NOP       EMIT $80
01B: 0082 F8C1 0080
                    (1002) S1ACRC MPC     RF 15 AND RCM => RF 15 ;
```



```
                    (1003)                NOP       EMIT $7F
01C: 0079 18C1 007F
                    (1004) S1BCRC MPC     TRN DR6 => RF 16
01D: 3481 1AC0 0000
                    (1005)        MPC     RF 16 AND RCM => RF 16 ;
                    (1006)                SCC       ACT 1 EMIT $80
01E: 0081 18BD 0080
                    (1007)        MPC     RF 15 OR DR7 => RF 15 ;
                    (1008)                NOP       JUMP ON CCBT TO RICRCR
01F: A079 1A4D A021
                    (1009)        MPC     NOP NOP   GOTO *+2
020: 0000 0040 8022
                    (1010) RICRCR MPC     RF 15 XOR RCM => RF 15 ;
                    (1011)                NOP       EMIT $3C
021: 0079 1841 003C
                    (1012)        MPC     NOP POP
022: 0000 0004 0000
                    (1013) *
                    (1014) * SUBROUTINE, DETECT READ STROBE DURING DELAY.
                    (1015) *
                    (1016) S3TRD  MPC     INC RF 7 => RF 7
023: 0039 0840 0000
                    (1017)        MPC     INC RF 8 => RF 8
024: 0041 0840 0000
                    (1018) S3TRD1 MPC     DEC RF 5 => RF 5 ;
                    (1019)                SCC       JUMP ON DIF3 TO RSDET
025: 0029 07BC F82C
                    (1020)        MPC     CON ZERO => DR6 ;
                    (1021)                NOP       JUMP ON NOT CCAEZ TO S3TRD1
026: 0002 D9C0 6425
                    (1022)        MPC     DEC RF 7 => RF 7 ;
                    (1023)                SCC       JUMP ON DIF3 TO RSDET
027: 0039 07BC F82C
                    (1024)        MPC     NOP NOP   JUMP ON NOT CCAEZ TO S3TRD1
028: 0000 0040 6425
                    (1025)        MPC     DEC RF 8 => RF 8 ;
                    (1026)                SCC       JUMP ON DIF3 TO RSDET
029: 0041 07BC F82C
```

```
                    (1027)          MPC     NOP NOP   JUMP ON NOT CCAEZ TO S3TRD1
02A: 0000 0040 6425
                    (1028)          MPC     CON ZERO => RF 8 POP
02B: 0041 1984 0000
                    (1029) RSDET    MPC     TRN DR5 => (RF 1,DR6)
02C: 3008 DAC0 0000
                    (1030)          MPC     TRN DB8 => (RF 12,DR7) ;
                    (1031)                  NOP       GOTO *-2
02D: 3C63 FAC0 802B
                    (1032) *
                    (1033) * SUBROUTINE. TAPE MOTION STOP DELAY
                    (1034) *
                    (1035) S4TSD    MPC     CON ZERO => NOP ;
                    (1036)                  IDR7       JUMP ON NOT DR7C0 TO S4TSD
02E: 0000 1990 402E
                    (1037)          MPC     TRN DR4 => NOP ;
                    (1038)                  SCC       ACT 3
02F: 2C00 1ABD 2000
                    (1039)          MPC     DEC RF 7 => RF 7 ;
                    (1040)                  SCC       JUMP ON CCBT TO BEOTSS
030: 0039 07BC A032
                    (1041)          MPC     NOP NOP   GOTO *+2
031: 0000 0040 8033
                    (1042) BEOTSS MPC       RF 4 OR RCM => RF 4 ;
                    (1043)                  NOP       EMIT $20
032: 0021 1A41 0020
                    (1044)          MPC     CON ZERO => NOP ;
                    (1045)                  NOP       JUMP ON OTAF TO S4END
033: 0000 19C0 8C37
                    (1046) BSPDO    MPC     CON ZERO => NOP ;
                    (1047)                  NOP       JUMP ON NOT CCAEZ TO S4TSD
034: 0000 19C0 642E
                    (1048)          MPC     DEC RF 8 => RF 8 ;
                    (1049)                  SCC
035: 0041 07BC 0000
                    (1050)          MPC     NOP CD13  JUMP ON NOT CCAEZ TO S4TSD
036: 0000 0058 642E
                    (1051) S4END    MPC     NOP POP
```



```
037: 0000 0004 0000
                    (1052) *
                    (1053) * SUBROUTINE 5. TEST FOR R.A.W. DATA
                    (1054) *
                    (1055) S5RAW    MPC     CON ZERO => NOP ;
                    (1056)                  NOP       JUMP ON NOT DIF3 TO WTPR
038: 0000 19C0 783F
                    (1057)          MPC     DEC RF 13 => RF 13 ;
                    (1058)                  CDI3      JUMP ON DIF2 TO WBCDP
039: 0069 07D8 F43C
                    (1059)          MPC     CON ZERO => NOP ;
                    (1060)                  NOP       JUMP ON DIFP TO WRAWE
03A: 0000 19C0 FC3D
                    (1061)          MPC     CON ZERO => NOP ;
                    (1062)                  CDIP      GOTO WRAWD
03B: 0000 19DC 803E
                    (1063) WBCDP    MPC     CON ZERO => NOP ;
                    (1064)                  NOP       JUMP ON DIFP TO *-1
03C: 0000 19C0 FC3B
                    (1065) WRAWE    MPC     RF 3 OR RCM => RF 3 ;
                    (1066)                  CDIP      EMIT $02
03D: 0019 1A5D 0002
                    (1067) WRAWD    MPC     NOP POP
03E: 0000 0004 0000
                    (1068) WTPR     MPC     CON ZERO => NOP
03F: 0000 19C0 0000
                    (1069)          MPC     CON ZERO => NOP
040: 0000 19C0 0000
                    (1070)          MPC     CON ZERO => NOP ;
                    (1071)                  NOP       GOTO WRAWD
041: 0000 19C0 803E
                    (1072) *
                    (1073) * THIS ROUTINE SETS UP CHANNEL NUMBER
                    (1074) *
                    (1075) BCHAN    MPC     TRN  DRL => RF 24
042: 50C1 1AC0 0000
                    (1076)          MPC     TRN  DRR => RF 25
043: 40C9 1AC0 0000
```



```
                    (1077) BMRDY    MPC     CON ZERO => (RF 8,SRL) ;
                    (1078)                  CB        JUMP ON DIF2 TO BCYCLE
044: 0045 0998 F5DC
                    (1079) BTSD     MPC     INC RF 8 => RF 8 ;
                    (1080)                  PSH       GOTO S4TSD
045: 0041 0808 802E
                    (1081)          MPC     NOP NOP   JUMP ON OTAF TO BSID
046: 0000 0040 8C09
                    (1082)          MPC     NOP NOP   GOTO BCYCLE
047: 0000 0040 81DC
                    (1083) *
                    (1084) * THIS ROUTINE SETS UP INTERRUPT VECTOR
                    (1085) *
                    (1086) BVECT    MPC     TRN  DRL => RF 31
048: 50F9 1AC0 0000
                    (1087)          MPC     TRN  DRR => RF 27 ;
                    (1088)                  NOP       GOTO BMRDY
049: 40D9 1AC0 8044
                    (1089) *
                    (1090) * THIS ROUTINE DECODES MOTION OTA
                    (1091) *
                    (1092) BMOT     MPC     TRN DRR => RF 1
04A: 4009 1AC0 0000
                    (1093)          MPC     RF 1 AND RCM => DR3 ;
                    (1094)                  NOP       EMIT $0F
04B: 000A 78C1 000F
                    (1095)          MPC     TRN  DRL => RF 29 ;
                    (1096)                  SCC       ACT 1
04C: 50E9 1ABD 0000
                    (1097)          MPC     RF 21 PLUS SRL + 1 => SRL ;
                    (1098)                  NOP       JUMP ON CCBT TO BSEL
04D: 58AC C840 A1F0
                    (1099) *
                    (1100) * MOTION SETUP ORDER WAS NOT SELECT ORDER
                    (1101) *
                    (1102)          MPC     RF 30 MINUS  DRR => NOP ;
                    (1103)                  SCC       JUMP ON DIF2 TO OD3XX
04E: 40F9 0C8C F455
```



```
                    (1104)          MPC     TRN  DRR => RF 1 ;
                    (1105)                  NOP       JUMP ON CCAEZ TO OD3XX
04F: 4009 1AC0 E455
                    (1106)          MPC     RF 30 AND RCM => RF 30  NOP  EMIT $0F
050: 00F1 18C1 000F
                    (1107)          MPC     RF 1 AND RCM => DR6 ;
                    (1108)                  NOP       EMIT $0F
051: 000A 58C1 000F
                    (1109)          MPC     RF 30 MINUS DR6 => NOP ;
                    (1110)                  SCC
052: 34F0 0C8C 0000
                    (1111)          MPC     CON ZERO => NOP ;
                    (1112)                  NOP       JUMP ON NOT CCAEZ TO OD3XX
053: 0000 19C0 6455
                    (1113) BTDTO    MPC     NOP PSH   GOTO S4TSD
054: 0000 0008 802E
                    (1114) *
                    (1115) * ORDER DECODE STARTS HERE
                    (1116) *
                    (1117) OD3XX    MPC     TRN  DRR => (RF 30,DR6) ;
                    (1118)                  SCC       ACT 3
055: 40F3 DABD 2000
                    (1119)          MPC     RF 28 2 DR6 + L => RF 28 ;
                    (1120)                  NOP       JUMP ON CCBT TO OSTAT
056: 34E1 1940 A06C
                    (1121)          MPC     TRN RCM => (RF 22,DR7) ;
                    (1122)                  NOP       EMIT $15
057: 00B3 FAC1 0015
                    (1123)          MPC     DEC RF 22 => (RF 22,DR7) ;
                    (1124)                  SCC
058: 00B3 E7BC 0000
                    (1125)          MPC     CON ZERO => RFDR7 ;
                    (1126)                  NOP       JUMP ON NOT CCAEZ TO *-1
059: 0201 19C0 6458
                    (1127)          MPC     TRN RF 25 =>  ARR
05A: 00CC 3840 0000
                    (1128)          MPC     RF 24 AND RCM =>  ARL ;
                    (1129)                  NOP       EMIT $07
```

```
05B: 00C4 B8C1 0007
                    (1130)          MPC     RF 24 AND RCM =>  (RF 24,MR)  ;
                    (1131)                  NOP       EMIT $08
05C: 00C5 78C1 0008
                    (1132)          MPC     RF 24 OR RCM => (RF 24,MR) ;
                    (1133)                  NOP       EMIT 04
05D: 00C5 7A41 0004
                    (1134)          MPC     RF 29 AND RCM => DR7 ;
                    (1135)                  NOP       EMIT $01
05E: 00EA F8C1 0001
                    (1136)          MPC     TRN DR7 => RF 9   CD11
05F: A049 1ADD 0000
                    (1137)          MPC     TRN RF 29 => NOP ;
                    (1138)                  SCC       ACT 6
060: 00E8 183D 5000
                    (1139)          MPC     CON MINUS1 => RF 22 ;
                    (1140)                  CD12      JUMP ON CCBT TO 09TFM
061: 00B1 0654 A068
                    (1141)          MPC     TRN RCM => (RF 1,DR1) ;
                    (1142)                  NOP       EMIT $0F
062: 000B 3AC1 000F
                    (1143)          MPC     TRN RCM => RF 22 ;
                    (1144)                  NOP       EMIT $3F
063: 00B1 1AC1 003F
                    (1145)          MPC     RF 6 XOR RCM => RF 6 ;
                    (1146)                  NOP       EMIT $04
064: 0031 1B41 0004
                    (1147)          MPC     TRN RF 29 => NOP ;
                    (1148)                  SCC       ACT 5
065: 00E8 183D 4000
                    (1149)          MPC     CON ZERO => NOP ;
                    (1150)                  NOP       JUMP ON NOT CCBT TO OHIDN
066: 0000 19C0 2068
                    (1151)          MPC     CON ZERO => NOP ;
                    (1152)                  SDF2
067: 0000 19E4 0000
                    (1153) OHIDN    MPC     TRN DB7=> NOP ;
                    (1154)                  SCC       ACT 8
```



```
068: 3800 1ABD 7000
                    (1155)          MPC     NOP NOP   JUMP ON CCBT TO OSTAT
069: 0000 0040 A06C
                    (1156)          MPC     NOP  SDF1 GOTO OSTAT
06A: 0000 0060 806C
                    (1157) 09TFM    MPC     TRN RCM => (RF 1,DR1) ;
                    (1158)                  NOP       EMIT $13
06B: 000B 3AC1 0013
                    (1159) *
                    (1160) * STATUS OF SELECTED DRIVE DECODE ROUTINE
                    (1161) *
                    (1162) OSTAT    MPC     TRN DR4 => RF 4 ;
                    (1163)                  SCC       ACT 1
06C: 2C21 1ABD 0000
                    (1164)          MPC     CON ZERO => (RF 3,DR5)  ;
                    (1165)                  NOP       JUMP ON CCBT TO OWOXX
06D: 001B B9C0 A071
                    (1166)          MPC     TRN RF 4 => NOP ;
                    (1167)                  SCC       ACT 2
06E: 0020 183D 1000
                    (1168)          MPC     CON ZERO => NOP ;
                    (1169)                  NOP       JUMP ON NOT CCBT TO BINTR
06F: 0000 19C0 2016
                    (1170)          MPC     NOP NOP   GOTO OSTAT
070: 0000 0040 806C
                    (1171) OWOXX    MPC     TRN RF 30 => NOP ;
                    (1172)                  SCC       ACT 4
071: 00F0 183D 3000
                    (1173)          MPC     CON ZERO => DR2 ;
                    (1174)                  NOP       JUMP ON NOT CCBT TO OMOTN
072: 0002 59C0 20F3
                    (1175)          MPC     TRN RF 4 => NOP ;
                    (1176)                  SCC       ACT 6
073: 0020 183D 5000
                    (1177)          MPC     CON ZERO => NOP ;
                    (1178)                  NOP       JUMP ON CCBT TO BINTR
074: 0000 19C0 A016
                    (1179)          MPC     TRN RF 30 => DR3
```



```
075: 00F2 7840 0000
                    (1180)          MPC     TRN RF 29 => NOP ;
                    (1181)                  SCC       ACT 2
076: 00E8 183D 1000
                    (1182) *
                    (1183) * START OF WRITE RECORD AND WRITE FILE MARK ROUTINE
                    (1184) *
                    (1185)          MPC     TRN RCM => RF 7 ;
                    (1186)                  NOP       EMIT 29
077: 0039 1AC1 001D
                    (1187)          MPC     CON ZERO => NOP ;
                    (1188)                  NOP       JUMP ON CCBT TO WBOTT
078: 0000 19C0 A07C
                    (1189)          MPC     RF 6 OR RCM => RF 6 ;
                    (1190)                  NOP       EMIT $03
079: 0031 1A41 0003
                    (1191)          MPC     TRN RCM => RF 8 ;
                    (1192)                  NOP       EMIT 5
07A: 0041 1AC1 0005
                    (1193)          MPC     CON ZERO => RF 9  ;
                    (1194)                  NOP       GOTO WDELAY
07B: 0049 19C0 8084
                    (1195) WBOTT    MPC     TRN RF 4 => NOP ;
                    (1196)                  SCC       ACT 5
07C: 0020 183D 4000
                    (1197)          MPC     CON ZERO => NOP ;
                    (1198)                  SDRQ      JUMP ON CCBT TO WLDY
07D: 0000 19C8 A083
                    (1199)          MPC     TRN RCM => RF 7 ;
                    (1200)                  NOP       EMIT 120
07E: 0039 1AC1 0078
                    (1201)          MPC     TRN RF 29 => NOP ;
                    (1202)                  SCC       ACT 6
07F: 00E8 183D 5000
                    (1203)          MPC     INC RF 8 => RF 8 ;
                    (1204)                  NOP       JUMP ON CCBT TO WDELAY
080: 0041 0840 A084
                    (1205)          MPC     RF 7 PLUS RCM => RF 7 ;
```



```
                    (1206)                  NOP       EMIT 26
081: 0039 0341 001A
                    (1207)          MPC     NOP NOP   GOTO WDELAY
082: 0000 0040 8084
                    (1208) WLDY     MPC     TRN RCM => RF 8 ;
                    (1209)                  NOP       EMIT 46
083: 0041 1AC1 002E
                    (1210) WDELAY   MPC     NOP PSH   GOTO S4TSD
084: 0000 0008 802E
                    (1211)          MPC     TRN RF 29 => NOP ;
                    (1212)                  SCC       ACT 2
085: 00E8 183D 1000
                    (1213)          MPC     CON ZERO => NOP ;
                    (1214)                  CDIP      JUMP ON NOT CCBT TO WDXXX
086: 0000 19DC 20A9
                    (1215) WDMXT    MPC     CON ZERO => NOP ;
                    (1216)                  NOP       JUMP ON DRQDP TO WORE
087: 00C0 19C0 D490
                    (1217)          MPC     CON ZERO => NOP ;
                    (1218)                  NOP       JUMP ON EOR TO WLTW
088: 0000 19C0 E891
                    (1219)          MPC     TRN  DRR => RF 11
089: 4059 1AC0 0000
                    (1220)          MPC     TRN DRL => RF 10
08A: 5051 1AC0 0000
                    (1221)          MPC     CON ZERO => NOP ;
                    (1222)                  SDRQ
08B: 0000 19C8 0000
                    (1223) W2CT     MPC     TRN RF 29 => NOP ;
                    (1224)                  SCC       ACT 8
08C: 00F8 183D 7000
                    (1225)          MPC     TRN RF 22 => DR7 ;
                    (1226)                  NOP       JUMP ON CCBT TO W2CTP
08D: 0082 F840 A08F
                    (1227)          MPC     RF 11 AND DR7 => DR6 ;
                    (1228)                  NOP       GOTO WCRCC
08E: A05A D8C0 809A
                    (1229) W2CTP    MPC     RF 10 AND DR7 => DR6 ;
```

```
                    (1230)                  NOP       GOTO WCRCC
08F: A052 D8C0 809A
                    (1231) WORE   MPC       RF 4 OR RCM => RF 4 ;
                    (1232)                  NOP       EMIT $02
090: 0021 1A41 0002
                    (1233) WLTW   MPC       RF 6 OR RCM => RF 6 ;
                    (1234)                  NOP       EMIT $03
091: 0031 1A41 0003
                    (1235)        MPC       TRN  DRR => RF 11
092: 4059 1AC0 0000
                    (1236)        MPC       TRN DRL => RF 10 ;
                    (1237)                  CDEOR     GOTO W2CT
093: 5051 1ACC 808C
                    (1238) WBCD1  MPC       TRN DR6 => NOP ;
                    (1239)                  SCC
094: 3400 1ABC 0000
                    (1240)        MPC       CON ZERO => RF 2 ;
                    (1241)                  NOP       JUMP ON  CCAEZ TO **+2
095: 0011 19C0 E497
                    (1242)        MPC       TRN FRR => RF 2 ;
                    (1243)                  NOP       GOTO **+2
096: 6011 1AC0 8098
                    (1244)        MPC       TRN RCM => DR1 ;
                    (1245)                  NOP       EMIT $0A
097: 0002 3AC1 000A
                    (1246)        MPC       NOP PSH   GOTO S1ACRC
098: 0000 0008 801C
                    (1247)        MPC       NOP NOP   GOTO WIWBC
099: 0000 0040 809C
                    (1248) *
                    (1249) *  START OF ROUTINE TO FORM WRITE CRC CHARACTER
                    (1250) *
                    (1251) WCRCC  MPC       TRN DR6 => DR1 ;
                    (1252)                  SIPF      JUMP ON DIF2 TO WBCD1
09A: 3402 3AAC F494
                    (1253) WCRCI  MPC       RF 2 BRN FRR => (RF 2,DR7) ;
                    (1254)                  PSH       GOTO S1CRC
09B: 6013 FD08 8018
```



```
                    (1255) *
                    (1256) * END OF CRC ROUTINE. INCREMENT WRITE BYTE COUNTER.
                    (1257) *
                    (1258) WIWBC  MPC       RF 2 AND RCM => (RF 2,DR2) ;
                    (1259)                  NOP       EMIT $80
09C: 0013 58C1 0080
                    (1260)        MPC       NOP NOP   JUMP ON NOT DIF1 TO WHID
09D: 0000 0040 70A1
                    (1261)        MPC       TRN RCM => DR7 ;
                    (1262)                  NOP       EMIT $DF
09E: 0002 FAC1 00DF
                    (1263)        MPC       NOP PSH   GOTO S5RAW
09F: 0000 0008 8038
                    (1264)        MPC       NOP IDR7  JUMP ON NOT DR7C0 TO *
0A0: 0000 0010 40A0
                    (1265) WHID   MPC       TRN RCM => DR7 ;
                    (1266)                  NOP       EMIT $DC
0A1: 0002 FAC1 00DC
                    (1267)        MPC       INC RF 13 => RF 13 ;
                    (1268)                  PSH       GOTO S5RAW
0A2: 0069 0808 8038
                    (1269)        MPC       TRN DR4 => NOP ;
                    (1270)                  SCC       ACT 3
0A3: 2C00 1ABD 2000
                    (1271)        MPC       NOP NOP   JUMP ON CCBT TO WEOTS
0A4: 0000 0040 A0A6
                    (1272)        MPC       NOP NOP   GOTO **+2
0A5: 0000 0040 80A7
                    (1273) WEOTS  MPC       RF 4 OR RCM => RF 4 ;
                    (1274)                  NOP       EMIT $20
0A6: 0021 1A41 0020
                    (1275)        MPC       NOP  IDR7 JUMP ON NOT DR7C0 TO *
0A7: 0000 0010 40A7
                    (1276)        MPC       CON MINUS1 => NOP ;
                    (1277)                  PSH       GOTO S5RAW
0A8: 0000 0608 8038
                    (1278) *
                    (1279) * GENERATE WRITE DATA STROBE OR WRITE AMPLIFIER RESET STROBE ROUTINE
```



```
                    (1280) *
                    (1281) WDXXX  MPC       TRN RF 6 => NOP ;
                    (1282)                  SCC       ACT 5
0A9: 0030 183D 4000
                    (1283)        MPC       CON ZERO => NOP ;
                    (1284)                  NOP       JUMP ON CCBT TO WARS
0AA: 0000 19C0 A0AC
                    (1285)        MPC       INC RF 2 => (RF 2,DR2) ;
                    (1286)                  NOP       GOTO **+2
0AB: 0013 4840 80AD
                    (1287) WARS   MPC       RF 2 OR RCM => (RF 2,DR2) ;
                    (1288)                  NOP       EMIT $02
0AC: 0013 5A41 0002
                    (1289)        MPC       INC RF 5 => RF 5 ;
                    (1290)                  SCC       ACT 6
0AD: 0029 083D 5000
                    (1291)        MPC       TRN RF 22 => DR6 ;
                    (1292)                  NOP       JUMP ON NOT CCBT TO *-1
0AE: 00B2 0840 20AD
                    (1293)        MPC       RF 2 AND RCM => (RF 2,DR2) ;
                    (1294)                  NOP       EMIT $80
0AF: 0013 58C1 0080
                    (1295)        MPC       TRN RF 9 => NOP ;
                    (1296)                  SCC
0B0: 0048 183C 0000
                    (1297)        MPC       CON ZERO => RF 5 ;
                    (1298)                  NOP       JUMP ON CCAEZ TO WAWW
0B1: 0029 19C0 E4B5
                    (1299)        MPC       TRN RCM => DR7 ;
                    (1300)                  NOP       EMIT $F6
0B2: 0002 FAC1 00F6
                    (1301) WPAD6  MPC       RF 11 AND DR6 => DR6 ;
                    (1302)                  IDR7      JUMP ON NOT DR7C0 TO *
0B3: 345A D890 40B3
                    (1303)        MPC       DEC RF 9 => RF 9 ;
                    (1304)                  NOP       GOTO WCRCC
0B4: 0049 07C0 809A
                    (1305) *
```



```
                    (1306) * WHEN ALL WORD HAS BEEN WRITTEN, CONTROL JUMPS HERE
                    (1307) *
                    (1308) WAWW   MPC       TRN RF 6 => NOP ;
                    (1309)                  SCC       ACT 7
0B5: 0030 183D 6000
                    (1310)        MPC       CON MINUS1 => DR7 ;
                    (1311)                  NOP       JUMP ON CCBT TO WADW
0B6: 0002 E640 A0B9
                    (1312)        MPC       RF 29 AND RCM => DR7 ;
                    (1313)                  NOP       EMIT $01
0B7: 00EA F8C1 0001
                    (1314)        MPC       TRN DR7 => RF 9 ;
                    (1315)                  NOP       GOTO WDMXT
0B8: A049 1AC0 8087
                    (1316) *
                    (1317) * WHEN ALL DATA HAS BEEN WRITTEN, DO THIS ROUTINE
                    (1318) *
                    (1319) WADW   MPC       TRN RF 6 => NOP ;
                    (1320)                  SCC       ACT 6
0B9: 0030 183D 5000
                    (1321)        MPC       NOP ;
                    (1322)                  NOP       JUMP ON CCBT TO WLRCT
0BA: 0000 0040 A0C7
                    (1323)        MPC       RF 15 XOR RCM => DR1 ;
                    (1324)                  NOP       EMIT $D7
0BB: 007A 3B41 00D7
                    (1325)        MPC       RF 16 XOR RCM => DR6 ;
                    (1326)                  NOP       EMIT $80
0BC: 0082 DB41 0080
                    (1327)        MPC       TRN DR6 => (RF 2,DR2)
0BD: 3413 5AC0 0000
                    (1328) WCRCD  MPC       RF 5 PLUS RCM => RF 5 ;
                    (1329)                  NOP       EMIT 43
0BE: 0029 0341 002B
                    (1330) WRWD1  MPC       NOP PSH   GOTO S5RAW
0BF: 0000 0008 8038
                    (1331)        MPC       DEC RF 5 => RF 5 ;
                    (1332)                  SCC
```

```
0C0: 0029 07BC 0000
                    (1333)          MPC     CON ZERO => NOP ;
                    (1334)                  NOP         JUMP ON NOT CCAEZ TO *-2
0C1: 0000 19C0 64BF
                    (1335)          MPC     TRN RF 29 => NOP ;
                    (1336)                  SCC         ACT 2
0C2: 00E8 183D 1000
                    (1337)          MPC     RF 6 3 DR1 + 1 => RF 6 ;
                    (1338)                  NOP         JUMP ON CCBT TO WDXXX
0C3: 2031 09C0 A0A9
                    (1339)          MPC     CON ZERO => NOP ;
                    (1340)                  NOP         JUMP ON NOT DR7C0 TO WDXXX
0C4: 0000 19C0 40A9
                    (1341)          MPC     TRN RCM => RF 5 ;
                    (1342)                  NOP         EMIT 2
0C5: 0029 1AC1 0002
                    (1343)          MPC     NOP IDR7  GOTO WTHID
0C6: 0000 0010 80D5
                    (1344) *
                    (1345) * JUMP TO THIS ROUTINE WHEN CRCC HAS BEEN WRITTEN (9T) OR ALWAYS (7T)
                    (1346) *
                    (1347) WLRCT    MPC     TRN RF 6 => NOP ;
                    (1348)                  SCC         ACT 5
0C7: 0030 183D 4000
                    (1349)          MPC     NOP ;
                    (1350)                  IDR7        JUMP ON NOT CCBT TO WTHID
0C8: 0000 0010 20D5
                    (1351) *
                    (1352) * THIS ROUTINE STARTS WHEN LRCC HAS BEEN WRITTEN
                    (1353) *
                    (1354) WRAWRD   MPC     TRN RCM => RF 7 ;
                    (1355)                  NOP         EMIT $19
0C9: 0039 1AC1 0019
                    (1356)          MPC     CON ZERO => RF 8 ;
                    (1357)                  PSH         GOTO S3TRD
0CA: 0041 1988 8023
                    (1358)          MPC     CON ZERO => NOP ;
                    (1359)                  NOP         JUMP ON DIF3 TO WNRAY
```



```
0CB: 0000 19C0 F8DD
                    (1360) WSTRA    MPC     RF 3 OR RCM => RF 3 ;
                    (1361)                  NOP         EMIT $40
0CC: 0019 1A41 0040
                    (1362) WSTPMO   MPC     RF 30 AND RCM => DR3 ;
                    (1363)                  CDI1        EMIT $0F
0CD: 00F2 78D1 000F
                    (1364)          MPC     RF 3 AND RCM => NOP ;
                    (1365)                  SCC         EMIT $FF
0CE: 0018 18BD 00FF
                    (1366)          MPC     CON ZERO => RF 8 ;
                    (1367)                  CDEOR   JUMP ON NOT CCAEZ TO BEOMI
0CF: 0041 19CC 64DA
                    (1368)          MPC     RF 4 AND RCM => DR6 ;
                    (1369)                  NOP         EMIT $F3
0D0: 0022 D8C1 00F3
                    (1370)          MPC     TRN DR6 => RF 1
0D1: 3409 1AC0 0000
                    (1371)          MPC     RF 1 MINUS RCM => NOP ;
                    (1372)                  SCC         EMIT $C0
0D2: 0008 0CBD 00C0
                    (1373)          MPC     CON ZERO => RF 8 ;
                    (1374)                  NOP         JUMP ON NOT CCAEZ TO BEOMI
0D3: 0041 19C0 64DA
                    (1375)          MPC     CON ZERO =>  SRL ;
                    (1376)                  NOP         GOTO BEOMI
0D4: 0004 D9C0 80DA
                    (1377) WTHID    MPC     NOP NOP   JUMP ON NOT DIF1 TO WCRCD
0D5: 0000 0040 70BE
                    (1378)          MPC     TRN RCM => RF 5 ;
                    (1379)                  NOP         EMIT 62
0D6: 0029 1AC1 003E
                    (1380)          MPC     NOP PSH   GOTO S5RAW
0D7: 0000 0008 8038
                    (1381)          MPC     NOP
0D8: 0000 0040 0000
                    (1382)          MPC     NOP NOP   GOTO WRWD1
0D9: 0000 0040 80BF
```



```
                    (1383) *
                    (1384) * TAPE MOTION HAS GONE FALSE, SET INTERRUPT REQUEST
                    (1385) *
                    (1386) BEOMI    MPC     TRN RF 27 =>  ARR ;
                    (1387)                  CDI2
0DA: 00DC 3854 0000
                    (1388) *
                    (1389) * SET UP 8.3 MS TAPE MOTION STOP DELAY
                    (1390) *
                    (1391)          MPC     TRN RCM => RF 7 ;
                    (1392)                  SIRQ        EMIT 107
0DB: 0039 1AC5 006B
                    (1393)          MPC     TRN RF 31 => ARL ;
                    (1394)                  CB      GOTO BTSD
0DC: 00FC BA18 8045
                    (1395) *
                    (1396) * ENTER HERE WHEN RAW DATA STROBES HAVE BEEN DETECTED FOLLOWING
                    (1397) * COMPLETION OF THE WRITE OPERATION
                    (1398) *
                    (1399) WNRAY    MPC     TRN RF 29 => NOP ;
                    (1400)                  SCC         ACT 2
0DD: 00E8 183D 1000
                    (1401)          MPC     CON ZERO => NOP ;
                    (1402)                  NOP         JUMP ON NOT CCBT TO WFMDO
0DE: 0000 19C0 20E9
                    (1403) WCRAWD   MPC     NOP PSH   GOTO S5RAW
0DF: 0000 0008 8038
                    (1404)          MPC     CON ZERO => RF 5 ;
                    (1405)                  NOP         JUMP ON NOT DIF1 TO WDGTO
0E0: 0029 19C0 70E2
                    (1406)          MPC     TRN RCM => RF 5 ;
                    (1407)                  NOP         EMIT 30
0E1: 0029 1AC1 001E
                    (1408) WDGTO    MPC     RF 5 PLUS RCM => RF 5 ;
                    (1409)                  NOP         EMIT 69
0E2: 0029 0341 0045
                    (1410)          MPC     DEC RF 5 => RF 5 ;
                    (1411)                  SCC         JUMP ON DIF3 TO WCRAWD
```



```
0E3: 0029 07BC F8DF
                    (1412)          MPC     TRN RF 13 => NOP ;
                    (1413)                  SCC         JUMP ON NOT CCAEZ TO *-1
0E4: 0068 183C 64E3
                    (1414)          MPC     CON ZERO => RF 8 ;
                    (1415)                  NOP         JUMP ON NOT CCAEZ TO WRAWES
0E5: 0041 19C0 64F1
                    (1416) WSTPDY   MPC     TRN RCM => RF 7 ;
                    (1417)                  NOP         EMIT 21
0E6: 0039 1AC1 0015
                    (1418)          MPC     INC RF 8 => RF 8 ;
                    (1419)                  PSH         GOTO S4TSD
0E7: 0041 0808 802E
                    (1420)          MPC     CON ZERO => NOP ;
                    (1421)                  NOP         GOTO WSTPMO
0E8: 0000 19C0 80CD
                    (1422) *
                    (1423) * WRITE FILE MARK ENTERS HERE TO CHECK RAW DATA
                    (1424) *
                    (1425) WFMDO    MPC     TRN RF 29 => NOP ;
                    (1426)                  SCC         ACT 6
0E9: 00E8 183D 5000
                    (1427)          MPC     CON ZERO => NOP ;
                    (1428)                  CDI3        JUMP ON CCBT TO WFM9TT
0EA: 0000 19D8 A0ED
                    (1429)          MPC     RF 1 MINUS RCM => NOP ;
                    (1430)                  SCC         EMIT $0F
0EB: 0008 0CBD 000F
                    (1431)          MPC     CON ZERO => NOP ;
                    (1432)                  NOP         GOTO *+2
0EC: 0000 19C0 80EE
                    (1433) WFM9TT   MPC     RF 1 MINUS RCM => NOP ;
                    (1434)                  SCC         EMIT $13
0ED: 0008 0CBD 0013
                    (1435)          MPC     CON ZERO => NOP ;
                    (1436)                  NOP         JUMP ON NOT CCAEZ TO WRAWES
0EE: 0000 19C0 64F1
                    (1437)          MPC     TRN RF 12 => NOP ;
```

```
                    (1438)                  SCC       ACT 7
0EF: 0060 183D 6000
                    (1439)          MPC     CON ZERO => RF 8 ;
                    (1440)                  NOP       JUMP ON NOT CCBT TO WSTPDY
0F0: 0041 19C0 20E6
                    (1441) WRAWES   MPC     RF 3 OR RCM => RF 3 ;
                    (1442)                  NOP       EMIT $02
0F1: 0019 1A41 0002
                    (1443)          MPC     CON ZERO => NOP ;
                    (1444)                  NOP        GOTO WSTPDY
0F2: 0000 19C0 80E6
                    (1445) *
                    (1446) * ORDER DECODE CONTINUES HERE FOR ALL EXCEPT WRITE ORDERS
                    (1447) *
                    (1448) OMOTN    MPC     TRN RF 30 => DR3 ;
                    (1449)                  SCC       ACT 3
0F3: 00F2 783D 2000
                    (1450)          MPC     TRN RF 1 => DR6 ;
                    (1451)                  NOP       JUMP ON CCBT TO ORWND
0F4: 000A D840 A1B7
                    (1452)          MPC     TRN RF 29 => NOP ;
                    (1453)                  SCC       ACT 2
0F5: 00E8 183D 1000
                    (1454)          MPC     TRN RCM => RF 7 ;
                    (1455)                  NOP       EMIT 86
0F6: 0039 1AC1 0056
                    (1456)          MPC     TRN DR6 => RF 0 ;
                    (1457)                  NOP       JUMP ON NOT CCBT TO BRBFFF
0F7: 3401 1AC0 2185
                    (1458)          MPC     TRN RF 30 => NOP ;
                    (1459)                  SCC       ACT 1
0F8: 00F0 183D 0000
                    (1460)          MPC     CON ZERO => NOP ;
                    (1461)                  NOP       JUMP ON NOT CCBT TO BRBFFF
0F9: 0000 19C0 2185
                    (1462)          MPC     RF 24 OR RCM =>  MR ;
                    (1463)                  NOP       EMIT $10
0FA: 00C4 7A41 0010
```



```
                    (1464) *
                    (1465) * START OF READ RECORD, READ RECORD AND CORRECT, FORWARD RECORD
                    (1466) * ROUTINE
                    (1467) *
                    (1468)          MPC     TRN RF 4 => NOP ;
                    (1469)                  SCC       ACT 5
0FB: 0020 183D 4000
                    (1470)          MPC     NOP NOP   JUMP ON NOT CCBT TO RSDLY
0FC: 0000 0040 20FE
                    (1471)          MPC     TRN RCM => RF 8 ;
                    (1472)                  NOP       EMIT 01
0FD: 0041 1AC1 0001
                    (1473) RSDLY    MPC     INC RF 8 => RF 8 ;
                    (1474)                  PSH       GOTO S4TSD
0FE: 0041 0808 802E
                    (1475)          MPC     TRN RCM => RF 8 ;
                    (1476)                  CDIP      EMIT 26
0FF: 0041 1ADD 001A
                    (1477)          MPC     NOP PSH   GOTO S3TRD
100: 0000 0008 8023
                    (1478)          MPC     CON ZERO => RF 22 ;
                    (1479)                  NOP       JUMP ON NOT DIF3 TO WSTRA
101: 00B1 19C0 78CC
                    (1480) RDAT     MPC     NOP CDI3  JUMP ON DIF2 TO RBCDM
102: 0000 0058 F508
                    (1481) RBINM    MPC     NOP NOP   JUMP ON NOT DIFP TO RFMVER
103: 0000 0040 7D0B
                    (1482) RTCOR    MPC     TRN RF 29 => NOP ;
                    (1483)                  SCC       ACT 4
104: 00E8 183D 3000
                    (1484)          MPC     NOP NOP   JUMP ON NOT CCBT TO RVPE1
105: 0000 0040 210A
                    (1485)          MPC     RF 26 XOR DR6 => DR6
106: 34D2 DB40 0000
                    (1486)          MPC     RF 23 XOR DR7 => DR7 ;
                    (1487)                  NOP       GOTO RFMVER
107: A0BA FB40 810B
                    (1488) RBCDM    MPC     NOP NOP   JUMP ON DIFP TO RFMVER
```



```
10R: 0000 0040 FD0B
                    (1489)          MPC     NOP NOP   GOTO RTCOR
109: 0000 0040 8104
                    (1490) RVPE1    MPC     RF 3 OR RCM => RF 3 ;
                    (1491)                  NOP       EMIT $80
10A: 0019 1A41 0080
                    (1492) RFMVER   MPC     RF 0 MINUS DR6 => NOP ;
                    (1493)                  SCC
10B: 3400 0CBC 0000
                    (1494)          MPC     INC RF 22 => RF 22 ;
                    (1495)                  NOP       JUMP ON NOT CCAEZ TO RLRCUP
10C: 00B1 0840 6510
                    (1496)          MPC     TRN DR7 => NOP ;
                    (1497)                  SCC       ACT 7
10D: A000 1ABD 6000
                    (1498)          MPC     NOP NOP   JUMP ON CCBT TO RLRCUP
10E: 0000 0040 A110
                    (1499)          MPC     INC RF 13 => RF 13
10F: 0069 0840 0000
                    (1500) RLRCUF   MPC     RF 19 XOR DR6 => RF 19
110: 3499 1B40 0000
                    (1501)          MPC     RF 20 XOR DR7 => RF 20 ;
                    (1502)                  NOP       JUMP ON NOT DIF2 TO REOTD
111: A0A1 1B40 7515
                    (1503)          MPC     RF 1 MINUS RCM => NOP ;
                    (1504)                  SCC       EMIT $0A
112: 0008 0CBD 000A
                    (1505)          MPC     NOP NOP   JUMP ON NOT CCAEZ TO REOTD
113: 0000 0040 6515
                    (1506)          MPC     CON ZERO => (RF 1,DR6)
114: 000B D9C0 0000
                    (1507) REOTD    MPC     TRN DR4 => NOP ;
                    (1508)                  SCC       ACT 3
115: 2C00 1ABD 2000
                    (1509)          MPC     TRN DR7 => RF 12 ;
                    (1510)                  NOP       JUMP ON NOT CCBT TO RTFR1
116: A061 1AC0 211A
                    (1511)          MPC     RF 4 OR RCM => RF 4 ;
```



```
                    (1512)                  NOP       EMIT $20
117: 0021 1A41 0020
                    (1513) RTFR1    MPC     TRN RF 29 => NOP ;
                    (1514)                  SCC       ACT 3
118: 00E8 183D 2000
                    (1515)          MPC     TRN DR6 => RF 1 ;
                    (1516)                  NOP       JUMP ON CCBT TO REPRR
119: 3409 1AC0 A126
                    (1517)          MPC     TRN RF 9 => NOP ;
                    (1518)                  SCC
11A: 0048 183C 0000
                    (1519)          MPC     RF 6 XOR RCM => RF 6 ;
                    (1520)                  NOP       EMIT $01
11B: 0031 1841 0001
                    (1521)          MPC     DEC RF 9 => RF 9 ;
                    (1522)                  NOP       JUMP ON CCAEZ TO RAWR
11C: 0049 07C0 E51E
                    (1523)          MPC     TRN DR6 => RF 10 ;
                    (1524)                  NOP       GOTO REPRR
11D: 3451 1AC0 8126
                    (1525) RAWR     MPC     TRN DR6 => RF 11
11E: 3459 1AC0 0000
                    (1526) RRQDMX   MPC     TRN RF 10 =>  DRL ;
                    (1527)                  NOP       JUMP ON DRQDP TO RDORS1
11F: 0054 9340 D525
                    (1528)          MPC     TRN RF 11 =>  DRR ;
                    (1529)                  NOP       JUMP ON NOT EOR TO RNEORS
120: 005C 1840 6924
                    (1530)          MPC     RF 3 OR RCM => RF 3 NOP EMIT $08
121: 0019 1A41 0008
                    (1531) RRCCR    MPC     RF 29 AND RCM => DR7 ;
                    (1532)                  NOP       EMIT $01
122: 00EA F8C1 0001
                    (1533)          MPC     TRN DR7 => RF 9 ;
                    (1534)                  NOP       GOTO REPRR
123: A049 1AC0 8126
                    (1535) RNEORS   MPC     NOP SDRQ  GOTO RRCCR
124: 0000 0048 8122
```

```
                    (1536) RDORS1 MPC     RF 4 OR RCM => RF 4 ;
                    (1537)                NOP       EMIT $02
125: 0021 1A41 0002
                    (1538) *
                    (1539) * UPDATE EPR ROUTINE STARTS HERE
                    (1540) *
                    (1541) REPRR  MPC     TRN RF 17 => DR6
126: 008A D840 0000
                    (1542)        MPC     TRN DR6RR => (RF 17,DR6)
127: 948B DAC0 0000
                    (1543)        MPC     TRN DR6 => RF 14
128: 3471 1AC0 0000
                    (1544)        MPC     RF 17 AND RCM => (RF 17,DR7) ;
                    (1545)                NOP       EMIT $7F
129: 008B F8C1 007F
                    (1546)        MPC     RF 18 OR DR7 => DR7
12A: A092 FA40 0000
                    (1547)        MPC     TRN DR7 => RF 17 ;
                    (1548)                NOP       JUMP ON DIFP TO REPPI
12B: A089 1AC0 FD2E
                    (1549)        MPC     RF 14 AND RCM => DR7 ;
                    (1550)                SCC       ACT 1  EMIT $80
12C: 0072 F8BD 0080
                    (1551)        MPC     NOP NOP   GOTO REPPI+1
12D: 0000 0040 812F
                    (1552) REPPI  MPC     RF 14 7 RCM + L => DR7 ;
                    (1553)                SCC       ACT 1  EMIT $80
12E: 0072 FBBD 0080
                    (1554)        MPC     TRN DR7 => RF 18 ;
                    (1555)                CDIP      JUMP ON NOT CCBT TO *+2
12F: A091 1ADC 2131
                    (1556)        MPC     RF 17 XOR RCM => RF 17 ;
                    (1557)                NOP       EMIT $3C
130: 0089 1B41 003C
                    (1558)        MPC     TRN RF 12 => NOP ;
                    (1559)                SCC       ACT 7
131: 0060 183D 6000
                    (1560)        MPC     CON ZERO => (RF 12,DR7) ;
```



```
                    (1561)                NOP       JUMP ON NOT CCBT TO *+2
132: 0063 F9C0 2134
                    (1562)        MPC     TRN RCM => (RF 12,DR7) ;
                    (1563)                NOP       EMIT $80
133: 0063 FAC1 0080
                    (1564)        MPC     TRN RF 1 => DR6 ;
                    (1565)                PSH       GOTO S1CRC
134: 000A D808 8018
                    (1566) *
                    (1567) * ENTER HERE AFTER COMPLETION OF CRC UPDATE
                    (1568) *
                    (1569) RECRCR MPC     TRN RF 6 => NOP ;
                    (1570)                SCC       ACT 4
135: 0030 183D 3000
                    (1571)        MPC     CON ZERO => RF 5 ;
                    (1572)                NOP       JUMP ON CCBT TO RCRCTR
136: 0029 19C0 A14E
                    (1573)        MPC     NOP NOP   JUMP ON NOT DIF1 TO *+2
137: 0000 0040 7139
                    (1574)        MPC     TRN RCM => RF 5 ;
                    (1575)                NOP       EMIT 50
138: 0029 1AC1 0032
                    (1576)        MPC     RF 5 PLUS RCM => RF 5 ;
                    (1577)                NOP       EMIT 113
139: 0029 0341 0071
                    (1578) *
                    (1579) * START TWO AND A HALF FRAME GAP DETECTION
                    (1580) *
                    (1581)        MPC     CON ZERO => RF 7 ;
                    (1582)                PSH   GOTO S3TRD
13A: 0039 1988 8023
                    (1583)        MPC     CON ZERO => RF 7 ;
                    (1584)                NOP       JUMP ON DIF3 TO RDAT
13B: 0039 19C0 F902
                    (1585)        MPC     CON ZERO => RF 5 ;
                    (1586)                NOP       JUMP ON NOT DIF1 TO *+2
13C: 0029 19C0 713E
                    (1587)        MPC     TRN RCM => RF 5 ;
```



```
                    (1588)                NOP       EMIT 60
13D: 0029 1AC1 003C
                    (1589)        MPC     RF 5 PLUS RCM => RF 5 ;
                    (1590)                NOP       EMIT 136
13E: 0029 0341 0088
                    (1591)        MPC     CON ZERO => DR7 ;
                    (1592)                PSH       GOTO S3TRD
13F: 0002 F988 8023
                    (1593) *
                    (1594) * CRCC (9T) OR LRCC (7T) HAS BEEN DETECTED
                    (1595) *
                    (1596)        MPC     TRN RF 29 => NOP ;
                    (1597)                SCC       ACT 8
140: 00E8 183D 7000
                    (1598)        MPC     TRN RF 9 => NOP ;
                    (1599)                SCC       JUMP ON NOT CCBT TO R9TT1
141: 0048 183C 2147
                    (1600)        MPC     NOP NOP   JUMP ON NOT CCAEZ TO R9TT1
142: 0000 0040 6547
                    (1601)        MPC     CON ZERO =>  DRR ;
                    (1602)                CDI3      JUMP ON DRQDP TO RDORS2
143: 0004 19D8 D546
                    (1603)        MPC     TRN RF 10 =>  DRL       NOP      JUMP ON EOR TO R9TT1
144: 0054 9840 E947
                    (1604)        MPC     NOP SDRQ  GOTO R9TT1
145: 0000 0048 8147
                    (1605) RDORS2 MPC     RF 4 OR RCM => RF 4 ;
                    (1606)                NOP       EMIT $02
146: 0021 1A41 0002
                    (1607) R9TT1  MPC     TRN RF 29 => NOP ;
                    (1608)                SCC       ACT 6
147: 00E8 183D 5000
                    (1609)        MPC     INC RF 9 => RF 9 ;
                    (1610)                NOP       JUMP ON NOT CCBT TO RLRCCK
148: 0049 0840 2159
                    (1611)        MPC     NOP NOP   JUMP ON DIF3 TO *+2
149: 0000 0040 F94B
                    (1612)        MPC     RF 6 OR RCM => RF 6 ;
```



```
                    (1613)                SDFP      EMIT 01
14A: 0031 1A6D 0001
                    (1614)        MPC     RF 6 XOR RCM => RF 6 ;
                    (1615)                SCC       ACT 8  EMIT $10
14B: 0031 183D 7010
                    (1616)        MPC     DEC RF 22 => RF 22 ;
                    (1617)                CDI3      JUMP ON NOT CCBT TO RBINM
14C: 00B1 07D8 2103
                    (1618)        MPC     NOP NOP   GOTO RBCDM
14D: 0000 0040 8108
                    (1619) *
                    (1620) * CHECK IF FINAL VALUE IN CRC REGISTER EQUALS MATCH PATTERN
                    (1621) *
                    (1622) RCRCTR MPC     TRN RF 16 => NOP ;
                    (1623)                SCC       ACT 1
14E: 0080 183D 0000
                    (1624)        MPC     TRN RF 15 => DR6 ;
                    (1625)                NOP       JUMP ON NOT CCBT TO RCRCER
14F: 007A D840 2153
                    (1626)        MPC     RF 15 XOR RCM => RF 15 ;
                    (1627)                NOP       EMIT $28
150: 0079 1B41 0028
                    (1628)        MPC     INC RF 15 => NOP ;
                    (1629)                SCC
151: 0078 083C 0000
                    (1630)        MPC     TRN DR6 => RF 15 ;
                    (1631)                NOP       JUMP ON CCAEZ TO RLRCCD
152: 3479 1AC0 E554
                    (1632) RCRCER MPC     RF 3 OR RCM => RF 3 ;
                    (1633)                NOP       EMIT $20
153: 0019 1A41 0020
                    (1634) RLRCCD MPC     TRN RCM => RF 5 ;
                    (1635)                NOP       EMIT $D6
154: 0029 1AC1 00D6
                    (1636)        MPC     CON ZERO => RF 7 ;
                    (1637)                PSH       GOTO S3TRD
155: 0039 1988 8023
                    (1638)        MPC     NOP NOP   JUMP ON DIF3 TO RLRCCK
```

```
156: 0000 0040 F959
                    (1639) RLRCER MPC     RF 3 OR RCM => RF 3 ;
                    (1640)                NOP       EMIT $10
157: 0019 1A41 0010
                    (1641)        MPC     NOP NOP   GOTO REORGD
158: 0000 0040 815D
                    (1642) *
                    (1643) * LRCC HAS BEEN DETECTED
                    (1644) *
                    (1645) RLRCCK MPC     RF 19 XOR DR6 => RF 19 ;
                    (1646)                SCC
159: 3499 1B3C 0000
                    (1647)        MPC     NOP CDI3  JUMP ON NOT CCAEZ TO RLRCER
15A: 0000 0058 6557
                    (1648)        MPC     RF 20 XOR DR7 => RF 20 ;
                    (1649)                SCC       ACT 7
15B: A0A1 1B3D 6000
                    (1650)        MPC     NOP NOP   JUMP ON CCBT TO RLRCER
15C: 0000 0040 A157
                    (1651) *
                    (1652) * START 16 FRAME GAP DETECTION
                    (1653) *
                    (1654) REORGD MPC     TRN RCM => RF 5 ;
                    (1655)                NOP       EMIT 224
15D: 0029 1AC1 00E0
                    (1656)        MPC     CON ZERO => RF 7 ;
                    (1657)                NOP       JUMP ON NOT DIF1 TO **2
15E: 0039 19C0 7160
                    (1658)        MPC     TRN RCM => RF 7 ;
                    (1659)                NOP       EMIT 2
15F: 0039 1AC1 0002
                    (1660)        MPC     RF 7 PLUS RCM => RF 7 ;
                    (1661)                CDI3      EMIT 3
160: 0039 0359 0003
                    (1662) RFGDY  MPC     DEC RF 5 => RF 5 ;
                    (1663)                SCC       JUMP ON DIF3 TO RFGD
161: 0029 07BC F979
                    (1664)        MPC     NOP NOP   JUMP ON NOT CCAEZ TO RFGDY
```



```
162: 0000 0040 6561
                    (1665) RFGDY1 MPC     DEC RF 7 => RF 7 ;
                    (1666)                SCC       JUMP ON DIF3 TO RFGD
163: 0039 07BC F979
                    (1667)        MPC     NOP NOP   JUMP ON NOT CCAEZ TO RFGDY
164: 0000 0040 6561
                    (1668)        MPC     RF 30 AND RCM => DR3 ;
                    (1669)                CDI1      EMIT $0F
165: 00F2 78D1 000F
                    (1670)        MPC     DEC RF 13 => RF 13 ;
                    (1671)                SCC
166: 0069 07BC 0000
                    (1672)        MPC     DEC RF 22 => RF 22 ;
                    (1673)                SCC       JUMP ON NOT CCAEZ TO RFIN
167: 00B1 07BC 656C
                    (1674)        MPC     NOP NOP   JUMP ON NOT CCAEZ TO RFIN
168: 0000 0040 656C
                    (1675)        MPC     TRN RF 3 => NOP ;
                    (1676)                SCC       ACT 4
169: 0018 183D 3000
                    (1677)        MPC     NOP NOP   JUMP ON CCBT TO RFIN
16A: 0000 0040 A16C
                    (1678)        MPC     INC RF 3 => RF 3 ;
                    (1679)                NOP       GOTO RFRC2
16B: 0019 0840 817B
                    (1680) RFIN   MPC     TRN RF 29 => NOP ;
                    (1681)                SCC       ACT 3
16C: 00E8 183D 2000
                    (1682)        MPC     CON ZERO => RF 23 ;
                    (1683)                NOP       JUMP ON CCBT TO RFRC2
16D: 00B9 19C0 A17B
                    (1684)        MPC     TRN RF 29 => NOP ;
                    (1685)                SCC       ACT 6
16E: 00E8 183D 5000
                    (1686)        MPC     CON ZERO => RF 26 ;
                    (1687)                NOP       JUMP ON NOT CCBT TO WSTPM0
16F: 00D1 19C0 20CD
                    (1688)        MPC     TRN RF 3 => NOP ;
```



```
                    (1689)                SCC       ACT 3
170: 0018 183D 2000
                    (1690)        MPC     INC RF 26 => RF 26 ;
                    (1691)                NOP       JUMP ON NOT CCBT TO WSTPM0
171: 00D1 0840 20CD
                    (1692) RTIER1 MPC     RF 15 XOR RCM => DR6 ;
                    (1693)                NOP       EMIT $D7
172: 007A 0B41 00D7
                    (1694)        MPC     RF 16 XOR RCM => DR7 ;
                    (1695)                NOP       EMIT $80
173: 0082 FB41 0080
                    (1696)        MPC     RF 18 XOR DR7 => NOP ;
                    (1697)                SCC       ACT 1
174: A090 1B3D 0000
                    (1698)        MPC     NOP NOP   JUMP ON CCBT TO RTIER2
175: 0000 0040 A179
                    (1699)        MPC     RF 17 MINUS DR6 => NOP ;
                    (1700)                SCC
176: 3488 0CBC 6060
                    (1701)        MPC     NOP NOP   JUMP ON NOT CCAEZ TO RTIER2
177: 0000 0040 657D
                    (1702)        MPC     RF 23 LS DR1 + 0 => RF 23 ;
                    (1703)                NOP       GOTO WSTPM0
178: 20B9 01C0 80CD
                    (1704) RFGD   MPC     RF 3 OR RCM => RF 3 ;
                    (1705)                CDI3      EMIT $08
179: 0019 1A59 0008
                    (1706)        MPC     NOP NOP   GOTO RFGDY1
17A: 0000 0040 8163
                    (1707) RFRC2  MPC     RF 3 AND RCM => RF 3 ;
                    (1708)                NOP       EMIT $49
17B: 0019 18C1 0049
                    (1709)        MPC     NOP NOP   GOTO WSTPM0
17C: 0000 0040 80C0
                    (1710) *
                    (1711) * PART OF TRACK IN ERROR ROUTINE
                    (1712) *
                    (1713) RTIER2 MPC     TRN RF 23 => NOP ;
```



```
                    (1714)                SCC       ACT 8
17D: 00B8 183D 7000
                    (1715)        MPC     CON ZERO => DR7 NOP   JUMP ON CCBT TO RUCED
17E: 0002 F9C0 A183
                    (1716)        MPC     CON ZERO => DR6 ;
                    (1717)                PSH       GOTO S1CRC
17F: 0002 D988 8018
                    (1718) RTIER3 MPC     RF 26 3 DR1 + 0 => RF 26 ;
                    (1719)                SCC
180: 20D1 01BC 0000
                    (1720)        MPC     NOP NOP   JUMP ON NOT CCAEZ TO RTIER1
181: 0000 0040 6572
                    (1721)        MPC     INC RF 23 => RF 23 ;
                    (1722)                NOP       GOTO RTIER1
182: 00B9 0840 8172
                    (1723) RUCED  MPC     RF 3 OR RCM => RF 3 ;
                    (1724)                NOP       EMIT $04
183: 0019 1A41 0004
                    (1725)        MPC     NOP NOP   GOTO WSTPM0
184: 0000 0040 80CD
                    (1726) *
                    (1727) * START OF BACK RECORD,BACK FILE AND FORWARD FILE ROUTINE
                    (1728) *
                    (1729) BRBFFF MPC     TRN RCM => RF 7 ;
                    (1730)                NOP       EMIT 65
185: 0039 1AC1 0041
                    (1731)        MPC     INC RF 8 => RF 8 ;
                    (1732)                PSH       GOTO S4TSD
186: 0041 0808 802E
                    (1733) BRSD   MPC     TRN RCM => RF 8 ;
                    (1734)                CDI3      EMIT 56
187: 0041 1AD9 0038
                    (1735)        MPC     CON ZERO => RF 13 ;
                    (1736)                PSH       GOTO S3TRD
188: 0069 1988 8023
                    (1737)        MPC     NOP NOP   JUMP ON NOT DIF3 TO WSTRA
189: 0000 0040 78CC
                    (1738) *
```

```
                    (1739) * FIRST READ STROBE HAS BEEN DETECTED (BACK REC,FILE ETC)
                    (1740) *
                    (1741)          MPC     TRN DR4 => NOP ;
                    (1742)                  SCC       ACT 3
18A: 2C00 1ABD 2000
                    (1743)          MPC     NOP CDI3   JUMP ON NOT CCBT TO *+2
18B: 0000 0058 218D
                    (1744)          MPC     RF 4 OR RCM => RF 4 ;
                    (1745)                  NOP       EMIT $20
18C: 0021 1A41 0020
                    (1746) BTFMOP   MPC     TRN RF 29 => NOP ;
                    (1747)                  SCC    ACT 2
18D: 00E8 183D 1000
                    (1748)          MPC     RF 0 MINUS DR6 => NOP ;
                    (1749)                  SCC       JUMP ON CCBT TO BRECOP
18E: 3400 0CBC A1AE
                    (1750)          MPC     CON ZERO => RF 7 ;
                    (1751)                  SDF2      JUMP ON NOT CCAEZ TO BRSD
18F: 0039 19E4 6587
                    (1752) BRDPT    MPC     TRN RF 12 => NOP ;
                    (1753)                  SCC       ACT 7
190: 0060 183D 6000
                    (1754)          MPC     NOP NOP   JUMP ON NOT CCBT TO BFMDET
191: 0000 0040 2180
                    (1755)          MPC     NOP NOP   JUMP ON DIF2 TO BRSD
192: 0000 0040 F587
                    (1756) B9TT     MPC     TRN RF 29 => NOP ;
                    (1757)                  SCC       ACT 6
193: 00E8 183D 5000
                    (1758)          MPC     NOP NOP   JUMP ON CCBT TO B6FDLY
194: 0000 0040 A1B3
                    (1759)          MPC     CON ZERO => RF 5 ;
                    (1760)                  NOP       JUMP ON NOT DIF1 TO *+2
195: 0029 19C0 7197
                    (1761)          MPC     TRN RCM => RF 5 ;
                    (1762)                  NOP       EMIT 40
196: 0029 1AC1 0028
                    (1763)          MPC     RF 5 PLUS RCM => RF 5 ;
```



```
                    (1764)                  NOP       EMIT 92
197: 0029 0341 005C
                    (1765) B60R2F   MPC     NOP PSH   GOTO S3TRD
198: 0000 0008 8023
                    (1766)          MPC     NOP NOP   JUMP ON DIF2 TO B5FDL2
199: 0000 0040 F5B5
                    (1767) B3FDY    MPC     CON ZERO => RF 5 ;
                    (1768)                  NOP       JUMP ON NOT DIF1 TO *+2
19A: 0029 19C0 719C
                    (1769)          MPC     TRN RCM => RF 5 ;
                    (1770)                  NOP       EMIT 60
19B: 0029 1AC1 003C
                    (1771)          MPC     RF 5 PLUS RCM => RF 5 ;
                    (1772)                  CDI3       EMIT 138
19C: 0029 0359 008A
                    (1773) BRSD1    MPC     CON ZERO => RF 7 ;
                    (1774)                  PSH       GOTO S3TRD
19D: 0039 1988 8023
                    (1775)          MPC     NOP NOP   JUMP ON NOT DIF3 TO BRSD
19E: 0000 0040 7987
                    (1776)          MPC     RF 0 MINUS DR6 => NOP ;
                    (1777)                  SCC
19F: 3400 0CBC 0000
                    (1778)          MPC     NOP NOP   JUMP ON NOT CCAEZ TO BFILOP
1A0: 0000 0040 65B1
                    (1779)          MPC     TRN RF 12 => NOP ;
                    (1780)                  SCC       ACT 7
1A1: 0060 183D 6000
                    (1781)          MPC     NOP NOP   JUMP ON CCBT TO BFILOP
1A2: 0000 0040 A1B1
                    (1782) B112FD   MPC     CON ZERO => RF 5 ;
                    (1783)                  NOP       JUMP ON NOT DIF1 TO *+2
1A3: 0029 19C0 71A5
                    (1784)          MPC     TRN RCM => RF 5 ;
                    (1785)                  NOP       EMIT 30
1A4: 0029 1AC1 001E
                    (1786)          MPC     RF 5 PLUS RCM => RF 5 ;
                    (1787)                  CDI3      EMIT 69
```



```
1A5: 0029 0359 0045
                    (1788)          MPC     CON ZERO => RF 7 ;
                    (1789)                  PSH       GOTO S3TRD
1A6: 0039 1988 8023
                    (1790)          MPC     INC RF 13 => RF 13 ;
                    (1791)                  NOP       JUMP ON DIF3 TO BFILOP
1A7: 0069 0840 F9B1
                    (1792)          MPC     RF 13 MINUS RCM => RF 13 ;
                    (1793)                  SCC       EMIT 2
1A8: 0069 0CBD 0002
                    (1794)          MPC     NOP NOP   JUMP ON NOT CCAEZ TO *+2
1A9: 0000 0040 65AB
                    (1795)          MPC     RF 3 OR RCM => RF 3 ;
                    (1796)                  NOP       EMIT 1
1AA: 0019 1A41 0001
                    (1797)          MPC     TRN RF 30 => NOP ;
                    (1798)                  SCC       ACT 1
1AB: 00F0 183D 0000
                    (1799)          MPC     CON ZERO => RF 8 ;
                    (1800)                  NOP       JUMP ON NOT CCBT TO WSTPDY
1AC: 0041 19C0 20E6
                    (1801)          MPC     NOP NOP   GOTO WSTPMO
1AD: 0000 0040 80ED
                    (1802) BRECOP   MPC     CON ZERO => RF 7 ;
                    (1803)                  CDI2      JUMP ON NOT CCAEZ TO B9TT
1AE: 0039 19D4 6593
                    (1804)          MPC     NOP NOP   GOTO BRDPT
1AF: 0000 0040 8190
                    (1805) BFMDET   MPC     INC RF 13 => RF 13 ;
                    (1806)                  NOP       GOTO B9TT
1B0: 0069 0840 8193
                    (1807) BFILOP   MPC     NOP NOP   JUMP ON DIF2 TO BRSD
1B1: 0000 0040 F587
                    (1808)          MPC     CON ZERO => RF 13 ;
                    (1809)                  NOP       GOTO B112FD
1B2: 0069 19C0 81A3
                    (1810) B6FDLY   MPC     TRN RCM => RF 5 ;
                    (1811)                  NOP       EMIT $14
```



```
1B3: 0029 1AC1 0014
                    (1812)          MPC     INC RF 7 => RF 7 ;
                    (1813)                  NOP       GOTO B60R2F
1B4: 0039 0840 8198
                    (1814) B5FDL2   MPC     NOP NOP   JUMP ON DIF3 TO BRSD
1B5: 0000 0040 F987
                    (1815)          MPC     NOP NOP   GOTO B3FDY
1B6: 0000 0040 819A
                    (1816) *
                    (1817) * REWIND ORDER STARTS HERE
                    (1818) *
                    (1819) ORWND    MPC     RF 30 AND RCM => DR6 ;
                    (1820)                  NOP       EMIT $0F
1B7: 00F2 D8C1 000F
                    (1821)          MPC     TRN RCM => DR7 ;
                    (1822)                  NOP       EMIT $FC
1B8: 0002 FAC1 00FC
                    (1823)          MPC     CON ZERO => RF 4 ;
                    (1824)                  IDR7      JUMP ON NOT DR7C0 TO *
1B9: 0021 1990 41B9
                    (1825)          MPC     RF 30 AND RCM => DR3 ;
                    (1826)                  SDF2       EMIT $0F
1BA: 00F2 78E5 000F
                    (1827)          MPC     RF 28 OR DR6 => RF 28 ;
                    (1828)                  NOP       GO TO BMRDY
1BB: 34E1 1A40 8044
                    (1829) *
                    (1830) *   POWER ON ROUTINE STARTS HERE
                    (1831) *
                    (1832) BPWR     MPC     TRN RCM => DR0 ;
                    (1833)                  NOP       EMIT $30
1BC: 0002 1AC1 0030
                    (1834)          MPC     TRN DRR => DR3
1BD: 4002 7AC0 0000
                    (1835)          MPC     RF 0 LS DR4 + 1 => RF 0 ;
                    (1836)                  PSH       GOTO S4TSD
1BE: 2C01 0988 802E
                    (1837)          MPC     TRN RCM => RF 8 ;
```

```
                    (1838)                  NOP       EMIT 56
1BF: 0041 1AC1 0038
                    (1839)          MPC     RF 0 LS DR4 + 0 => DR4 ;
                    (1840)                  PSH       GOTO S4TSD
1C0: 2C02 8188 802E
                    (1841)          MPC     TRN RCM => RF 8 ;
                    (1842)                  NOP       EMIT 56
1C1: 0041 1AC1 0038
                    (1843)          MPC     CON ZERO => DR4 ;
                    (1844)                  PSH       GOTO S4TSD
1C2: 0002 9988 802E
                    (1845)          MPC     TRN RCM => DR7 ;
                    (1846)                  NOP       EMIT $FD
1C3: 0002 FAC1 00FD
                    (1847)          MPC     TRN RCM => DR4 ;
                    (1848)                  NOP       EMIT $02
1C4: 0002 9AC1 0002
                    (1849)          MPC     NOP IDR7  JUMP ON NOT DR7C0 TO *
1C5: 0000 0010 41C5
                    (1850)          MPC     TRN RCM => DR0 ;
                    (1851)                  NOP       EMIT $E4
1C6: 0002 1AC1 00E4
                    (1852)          MPC     CON ZERO => DR4 ;
                    (1853)                  NOP       GOTO BMRDY
1C7: 0002 99C0 8044
                    (1854) *
                    (1855) * CONTINUATION OF OTA DECODES STARTS HERE
                    (1856) *
                    (1857) BHOUSE MPC       TRN  DRL => NOP ;
                    (1858)                  SCC       ACT 1
1C8: 5000 1ABD 0000
                    (1859)          MPC     TRN OFC => RF 0 NOP   JUMP ON CCBT TO BSTATI
1C9: 5C01 1AC0 A1D1
                    (1860)          MPC     TRN  DRL => NOP ;
                    (1861)                  SCC    ACT 2
1CA: 5000 1ABD 1000
                    (1862)          MPC     TRN MR => DR6 NOP   JUMP ON CCBT TO BIDI
1CB: 4C02 DAC0 A1D4
```



```
                    (1863)          MPC     TRN  DRL => NOP ;
                    (1864)                  SCC    ACT 3
1CC: 5000 1ABD 2000
                    (1865)          MPC     TRN RF 25 => DRR NOP   JUMP ON CCBT TO BCHANI
1CD: 00CC 1840 A1DB
                    (1866)          MPC     TRN  DRL => NOP ;
                    (1867)                  SCC       ACT 4
1CE: 5000 1ABD 3000
                    (1868)          MPC     TRN RF 31 => DRL ;
                    (1869)                  NOP       JUMP ON NOT CCBT TO BINTR
1CF: 00FC 9840 2016
                    (1870) *
                    (1871) * INA VECTOR ADDRESS
                    (1872) *
                    (1873)          MPC     TRN RF 27 => DRR ;
                    (1874)                  SIRDY      GOTO BMRDY
1D0: 00DC 1814 8044
                    (1875) *
                    (1876) * INA STATUS
                    (1877) *
                    (1878) BSTATI MPC       TRN RF 3 =>  DRL
1D1: 001C 9840 0000
                    (1879)          MPC     RF 4 AND RCM => RF 4 ;
                    (1880)                  NOP       EMIT $23
1D2: 0021 18C1 0023
                    (1881)          MPC     RF 4 OR DR4 => (RF 4, DRR) ;
                    (1882)                  SIRDY      GOTO BMRDY
1D3: 2C25 1A14 8044
                    (1883) *
                    (1884) * INA ID NUMBER
                    (1885) *
                    (1886) BIDI   MPC       TRN RCM =>  DRR ;
                    (1887)                  NOP       EMIT $0C
1D4: 0004 1AC1 000C
                    (1888)          MPC     RF 0 AND RCM => RF 0 ;
                    (1889)                  NOP       EMIT $C0
1D5: 0001 18C1 00C0
                    (1890)          MPC     TRN DR6RR => DR6
```



```
1D6: 9402 DAC0 0000
                    (1891)          MPC     RF 0 OR DR6RR => DR6
1D7: 9402 DA40 00C0
                    (1892)          MPC     TRN DR6RR => DR6
1D8: 9402 DAC0 0000
                    (1893)          MPC     TRN DR6RR => DR6
1D9: 9402 DAC0 0000
                    (1894)          MPC     TRN DR6RR => DRL ;
                    (1895)                  SIRDY      GOTO BMRDY
1DA: 9404 9A94 8044
                    (1896) *
                    (1897) * INA CHANNEL NUMBER
                    (1898) *
                    (1899) BCHANI MPC       TRN RF 24 =>  DRL ;
                    (1900)                  SIRDY      GOTO BMRDY
1DB: 00C4 9814 8044
                    (1901) *
                    (1902) * THIS ROUTINE IS THE IDLE LOOP WHEN TRANSPORT DELAY
                    (1903) *  HAS EXPIRED
                    (1904) *
                    (1905) BCYCLE MPC       TRN RCM => (RF 0,DR3) ;
                    (1906)                  NOP       EMIT $08
1DC: 0003 7AC1 0008
                    (1907)          MPC     CON ZERO => RF 1 ;
                    (1908)                  SDF2      JUMP ON OTAF TO BSID
1DD: 0009 19E4 8C09
                    (1909) BTRWD1 MPC       TRN RF 28 => NOP ;
                    (1910)                  SCC       ACT 5
1DE: 00E0 183D 4000
                    (1911)          MPC     TRN RF 0 => DR6 ;
                    (1912)                  NOP       JUMP ON NOT CCBT TO *+3
1DF: 0002 D840 21E2
                    (1913)          MPC     TRN DR4 => NOP ;
                    (1914)                  SCC       ACT 4
1E0: 2C00 1ABD 3000
                    (1915)          MPC     TRN RF 0 => DR7 ;
                    (1916)                  NOP       JUMP ON NOT CCBT TO BRWDF
1E1: 0002 F840 21EA
```



```
                    (1917)          MPC     TRN DR6RR => RF 0 ;
                    (1918)                  NOP       JUMP ON OTAF TO BTRWD3
1E2: 9401 1AC0 8DE7
                    (1919)          MPC     RF 0 AND RCM => (RF 0,DR3) ;
                    (1920)                  NOP       EMIT $0F
1E3: 0003 78C1 000F
                    (1921)          MPC     RF 28 3 DR1 + 0 => RF 28
1E4: 20E1 01C0 0000
                    (1922)          MPC     INC RF 1 => RF 1 ;
                    (1923)                  SCC       ACT 6
1E5: 0009 083D 5000
                    (1924)          MPC     NOP NOP   JUMP ON NOT CCBT TO BTRWD1
1E6: 0000 0040 21DE
                    (1925) BTRWD3 MPC       DEC RF 1 => RF 1 ;
                    (1926)                  SCC       ACT 1
1E7: 0009 07BD 0000
                    (1927)          MPC     TRN RF 28 => DR6 ;
                    (1928)                  NOP       JUMP ON CCBT TO BCYCLE
1E8: 00E2 D840 A1DC
                    (1929) BTRWD2 MPC       TRN DR6RR => (RF 28,DR6) ;
                    (1930)                  NOP       GOTO *-2
1E9: 94E3 DAC0 81E7
                    (1931) BRWDF  MPC       DEC RF 1 => RF 1 ;
                    (1932)                  SCC       ACT 1
1EA: 0009 07BD 0000
                    (1933)          MPC     TRN RF 28 => DR6 ;
                    (1934)                  SB       JUMP ON CCBT TO BSRWIS
1EB: 00E2 D838 A1ED
                    (1935)          MPC     TRN DR6RR => (RF 28,DR6) ;
                    (1936)                  NOP       GOTO BRWDF
1EC: 94E3 DAC0 81EA
                    (1937) BSRWIS MPC       RF 4 OR RCM => (RF 4,SRL) ;
                    (1938)                  NOP       EMIT $01
1ED: 0025 DA41 0001
                    (1939)          MPC     RF 28 XOR DR7 => RF 28 ;
                    (1940)                  NOP       JUMP ON OTAF TO BSID
1EE: A0E1 1B40 8C09
                    (1941)          MPC     NOP NOP   GOTO BINTR
```

```
1EF: 0000 0040 8016
                    (1942) BSEL   MPC     TRN DRR => RF 30 ;
                    (1943)                NOP       GOTO BMRDY
1F0: 40F1 1AC0 8044
          000761
```



```
B112FD   01A3  A 1783  1809
B3FDY    019A  A 1768  1815
B5FDL2   01B5  A 1766  1814
B6FDLY   01B3  A 1758  1811
B60R2F   0198  A 1765  1813
B9TT     0193  A 1757  1803  1806
BCHAN    0042  A 0975  1075
BCHANI   01DB  A 1865  1900
BCYCLE   01DC  A 1078  1082  1906  1928
BEGIN    0008  A 0964  0992
BEOMI    00DA  A 1367  1374  1376  1387
BEOTSS   0032  A 1040  1043
BFILOP   01B1  A 1778  1781  1791  1807
BFMDET   01B0  A 1754  1806
BHOUSE   01C8  A 0985  1858
BIDI     01D4  A 1862  1887
BINTR    0016  A 0990  1169  1178  1869  1941
BMOT     004A  A 0971  1092
BMRDY    0044  A 1078  1088  1828  1853  1874  1882  1895  1900  1943
BPWR     01BC  A 0989  1833
BRBFFF   0185  A 1457  1461  1730
BRDPT    0190  A 1753  1804
BRECOP   01AE  A 1749  1803
BRSD     0187  A 1734  1751  1755  1775  1807  1814
BRSD1    019D  A 1774
BRWDF    01EA  A 1916  1932  1936
BSEL     01F0  A 1098  1943
BSID     0009  A 0966  1081  1908  1940
BSPDO    0034  A 1047
BSRWIS   01ED  A 1934  1938
BSTATI   01D1  A 1859  1878
BTDTO    0054  A 1113
BTFMOP   018D  A 1747
BTRWD1   01DE  A 1910  1924
BTRWD2   01E9  A 1930
BTRWD3   01E7  A 1918  1926
BTSD     0045  A 1080  1394
BVECT    0048  A 0979  1086
```



```
INIT     0000  A 0941
O9TFM    006B  A 1140  1158
OD3XX    0055  A 1103  1105  1112  1118
OHIDN    0068  A 1150  1154
OMOTN    00F3  A 1174  1449
ORWND    01B7  A 1451  1820
OSTAT    006C  A 1120  1155  1156  1163  1170
OWOXX    0071  A 1165  1172
R9TT1    0147  A 1599  1600  1603  1604  1608
RAWR     011E  A 1522  1525
RBCDM    0108  A 1480  1488  1618
RBINM    0103  A 1481  1617
RCRCER   0153  A 1625  1633
RCRCTR   014E  A 1572  1623
RDAT     0102  A 1480  1584
RDORS1   0125  A 1527  1537
RDORS2   0146  A 1602  1606
RECRCR   0135  A 1570
REORGD   0150  A 1641  1655
REOTD    0115  A 1502  1505  1508
REPPI    012E  A 1548  1551  1553
REPRR    0126  A 1516  1524  1534  1541
RFGD     0179  A 1663  1666  1705
RFGDY    0161  A 1663  1664  1667
RFGDY1   0163  A 1666  1706
RFIN     016C  A 1673  1674  1677  1681
RFMVER   010B  A 1481  1487  1488  1493
RFRC2    017B  A 1679  1683  1708
RICRCR   0021  A 1008  1011
RLRCCD   0154  A 1631  1635
RLRCCK   0159  A 1610  1638  1646
RLRCER   0157  A 1640  1647  1650
RLRCUP   0110  A 1495  1498  1500
RNEORS   0124  A 1529  1535
RRCCR    0122  A 1532  1535
RRQDMX   011F  A 1527
RSDET    002C  A 1019  1023  1026  1029
RSDLY    00FE  A 1470  1474
```



```
RTCOR    0104  A 1483  1489
RTFR1    0118  A 1510  1514
RTIER1   0172  A 1693  1720  1722
RTIER2   017D  A 1698  1701  1714
RTIER3   0180  A 1719
RUCED    0183  A 1715  1724
RVPE1    010A  A 1484  1491
S1ACRC   001C  A 1003  1246
S1BCRC   001D  A 1004
S1CRC    0018  A 0997  1254  1565  1717
S3TRD    0023  A 1016  1357  1477  1582  1592  1637  1736  1765  1774
                1789
S3TRD1   0025  A 1019  1021  1024  1027
S4END    0037  A 1045  1051
S4TSD    002E  A 0954  1036  1036  1047  1050  1080  1113  1210  1419
                1474  1732  1836  1840  1844
S5RAW    0038  A 1056  1263  1268  1277  1330  1380  1403
W2CT     008C  A 1224  1237
W2CTP    008F  A 1226  1230
WADW     00B9  A 1311  1320
WARS     00AC  A 1284  1288
WAWW     00B5  A 1298  1309
WBCD1    0094  A 1239  1252
WBCDP    003C  A 1058  1064
WBOTT    007C  A 1188  1196
WCRAWD   00DF  A 1403  1411
WCRCC    009A  A 1228  1230  1252  1304
WCRCD    00BE  A 1329  1377
WCRCI    009B  A 1254
WDELAY   0084  A 1194  1204  1207  1210
WDGTO    00E2  A 1405  1409
WDMXT    0087  A 1216  1315
WDXXX    00A9  A 1214  1282  1338  1340
WEOTS    00A6  A 1271  1274
WFM9TT   00ED  A 1428  1434
WFMDO    00E9  A 1402  1426
WHID     00A1  A 1260  1266
WIWBC    009C  A 1247  1259
```

```
  WLDY      0083  A 1198  1209
  WLRCT     00C7  A 1322  1348
  WLTW      0091  A 1218  1234
  WNRAY     00DD  A 1359  1400
  WORE      0090  A 1216  1232
  WPAD6     00B3  A 1302
  WRAWD     003E  A 1062  1067  1071
  WRAWE     003D  A 1060  1066
  WRAWES    00F1  A 1415  1436  1442
  WRAWRD    00C9  A 1355
  WRWD1     00BF  A 1330  1382
  WSTPDY    00E6  A 1417  1440  1444  1800
  WSTPMO    00CD  A 1363  1421  1687  1691  1703  1709  1725  1801
  WSTRA     00CC  A 1361  1479  1737
  WTHID     00D5  A 1343  1350  1377
  WTPR      003F  A 1056  1068
MPC   [MACRO]
ALU$ [MACRO]
TRN$ [MACRO]
NOT$ [MACRO]
INC$ [MACRO]
DEC$ [MACRO]
CON$ [MACRO]
DEST$  [MACRO]
DST1$  [MACRO]
EMAC$  [MACRO]
PEQU$  [MACRO]
JMPF$  [MACRO]
BRAN$  [MACRO]
GOTO$  [MACRO]
PLUS$  [MACRO]
GEND$  [MACRO]
SETV$  [MACRO]
SAY1$  [MACRO]
ORG   [MACRO]
IDNT [MACRO]
NOP   [MACRO]
CNTV$  [MACRO]
```



```
CLST$  [MACRO]

0000 ERRORS (PMA-1080.015)
```

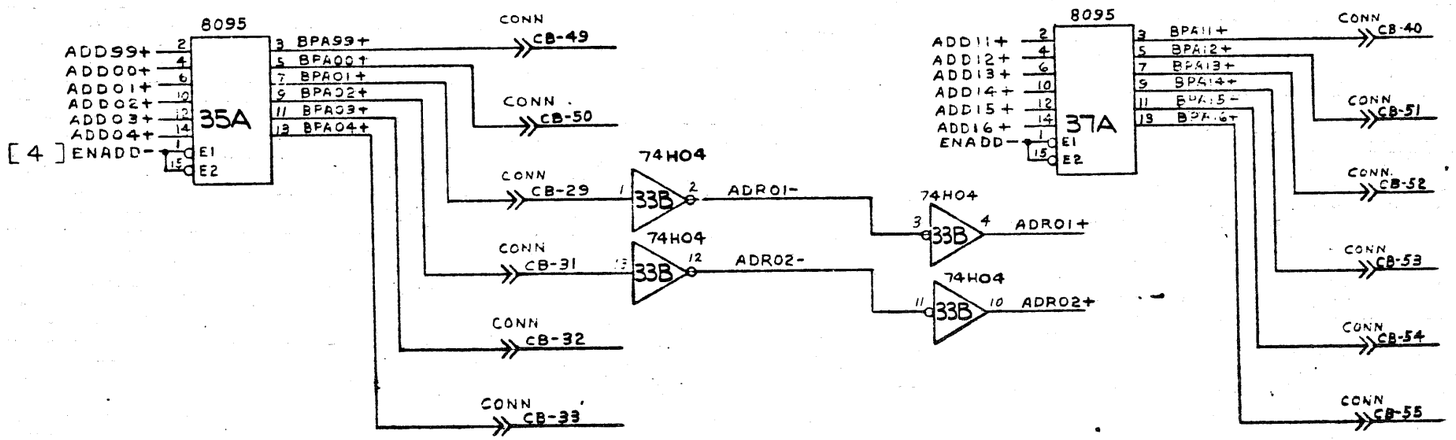
LTR	DATE	REVISION	DR.	CK.
			WJ2	JBM
			JVB	MDM

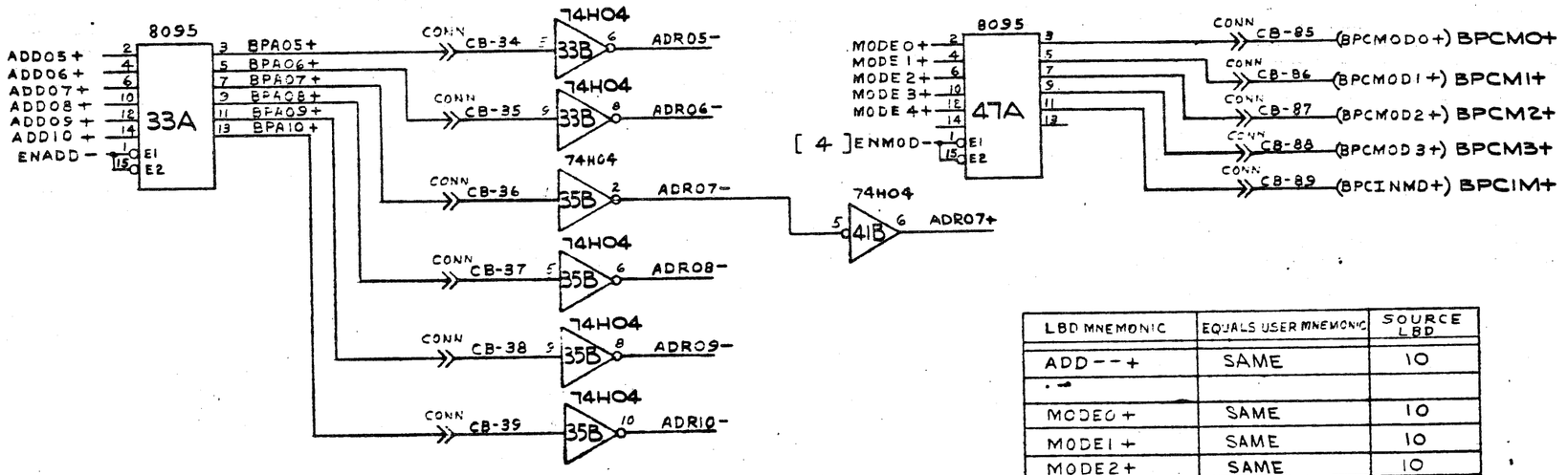
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28 A	28 B	28 C	29	30	31 A	31 B	31 C	32	32 A	32 B	32 C	33	33 A	33 B	33 C	34	35	35 A	36	36 A	36 B	36 C	DATE	ENGINEERING CHANGE NOTICE
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	10/16/74	RELEASED
	B							B				B																																					12/11/74	REVISED PER ECN 1502

REVISION LEVEL

MATERIAL	DWN F. Hagan 3/7/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK J. D'Amico 10/11/74	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG. D. Sandonato 10/10/74	REVISION STATUS SHEET MPC-2 E.V.
	APPRD J.D'M 10-9-74	
	USED ON NEXT ASSY 3155-002	SCALE SHEET 1 OF 36 · SIZE C · DWG. NO. LBD1829 · REV. B

PRIME COMPUTER, INC.





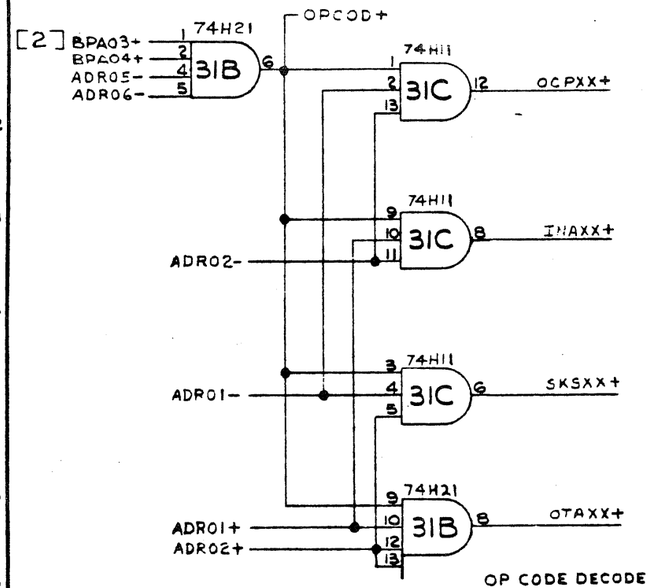
I/O BUS ADDRESS
DRIVERS & RECEIVERS

LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
ADD--+	SAME	10
MODE0+	SAME	10
MODE1+	SAME	10
MODE2+	SAME	10
MODE3+	SAME	10
MODE4+	SAME	10

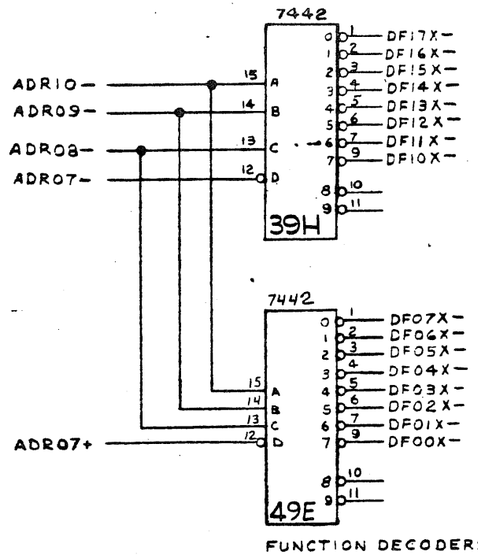
III-2

MATERIAL	DWN 3/13/73	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	I/O BUS INTERFACE LOGIC ADDRESS AND MODE LINES MPC2 (EV)
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	
	APPRD	
	USED ON	SCALE
	NEXT ASSY	SHEET OF
		SIZE C DWG. NO. LBD1829 REV. A

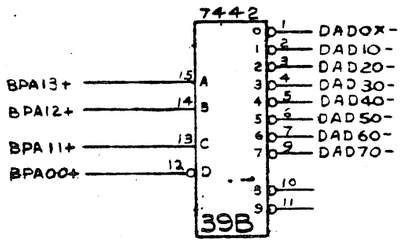
PDP-8/S

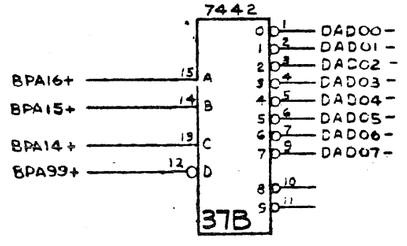


OP CODE DECODE

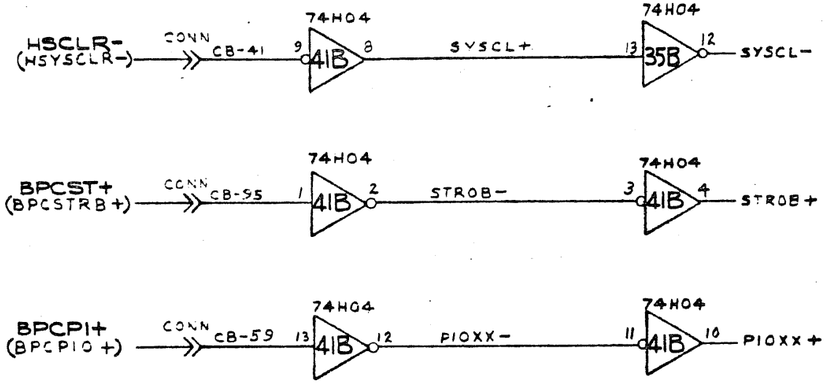


FUNCTION DECODERS





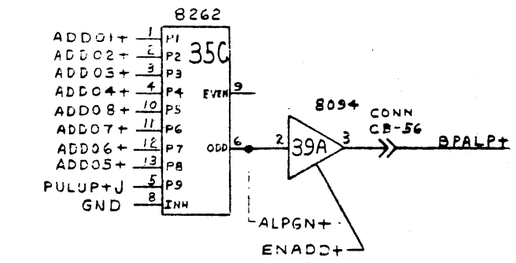
OCTAL ADDRESS DECODERS

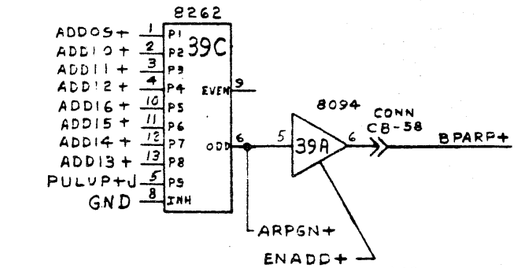


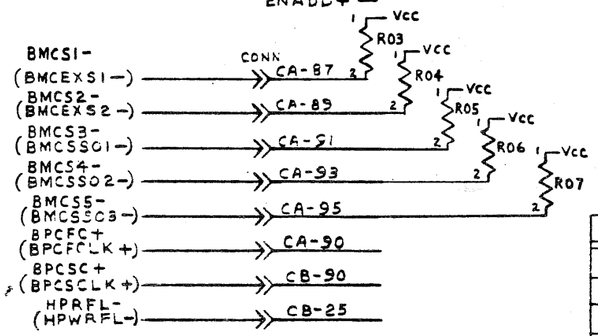
MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	I/O BUS INTERFACE LOGIC ADDRESS DECODING MPC2 (EV)
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 3 OF — SIZE C — DWG. NO. LBD1829 — REV —

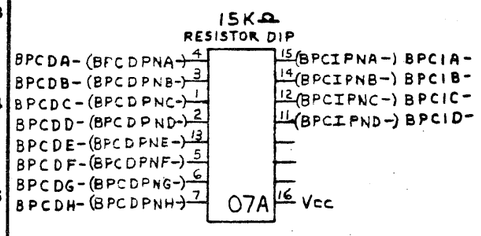
PUF-003

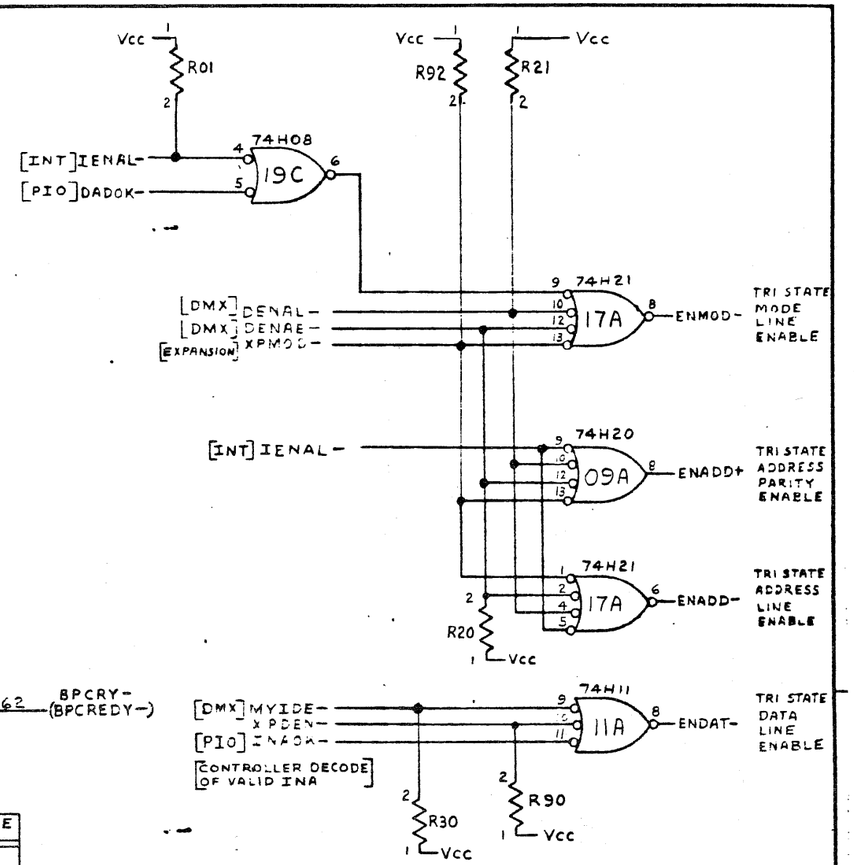
PRIME COMPUTER, INC.

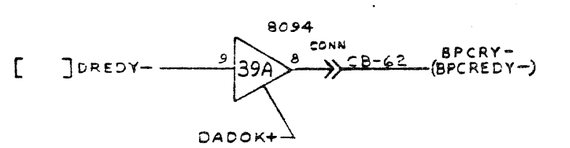






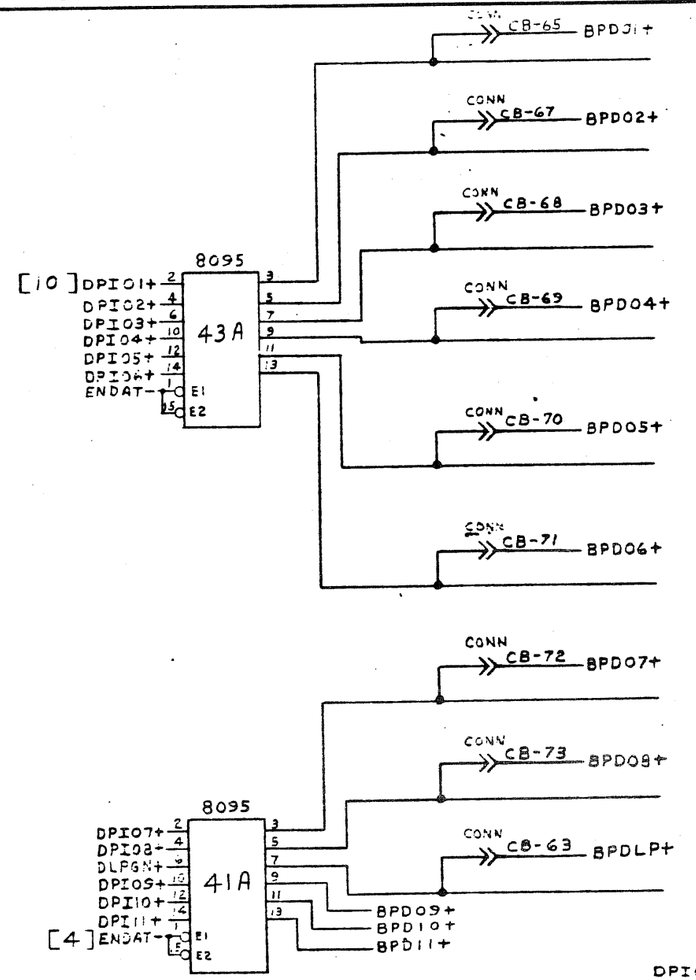


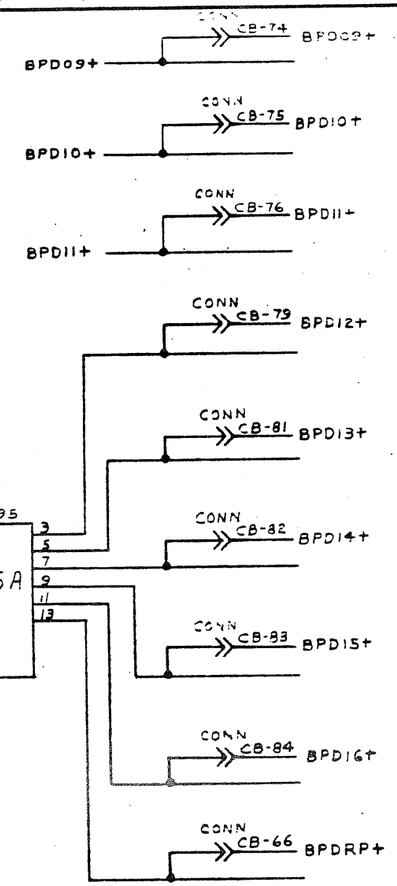


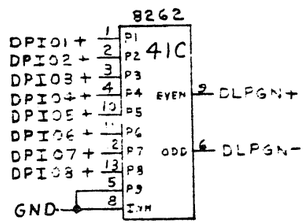


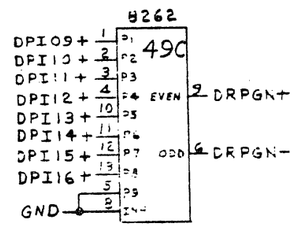
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
COCMD+	MOD14-	10
ADD--+	SAME	10
DADOK-	SAME	9
XPMOD-	NOT USED	—
XPDEN-	NOT USED	—
INAOK-	SAME	9
OTAOK+	SAME	9
XPDEE-	NOT USED	—
DREDY-	SAME	8
DADOK+	SAME	9

MATERIAL	DWN JH JK JR 3/15/73	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	I/O BUS INTERFACE LOGIC ADDRESS PARITY MPC2 EV
	APPRD	
	USED ON	SCALE / SIZE C / DWG. NO. LBD1829 / REV. A
	NEXT ASSY	SHEET 4 OF







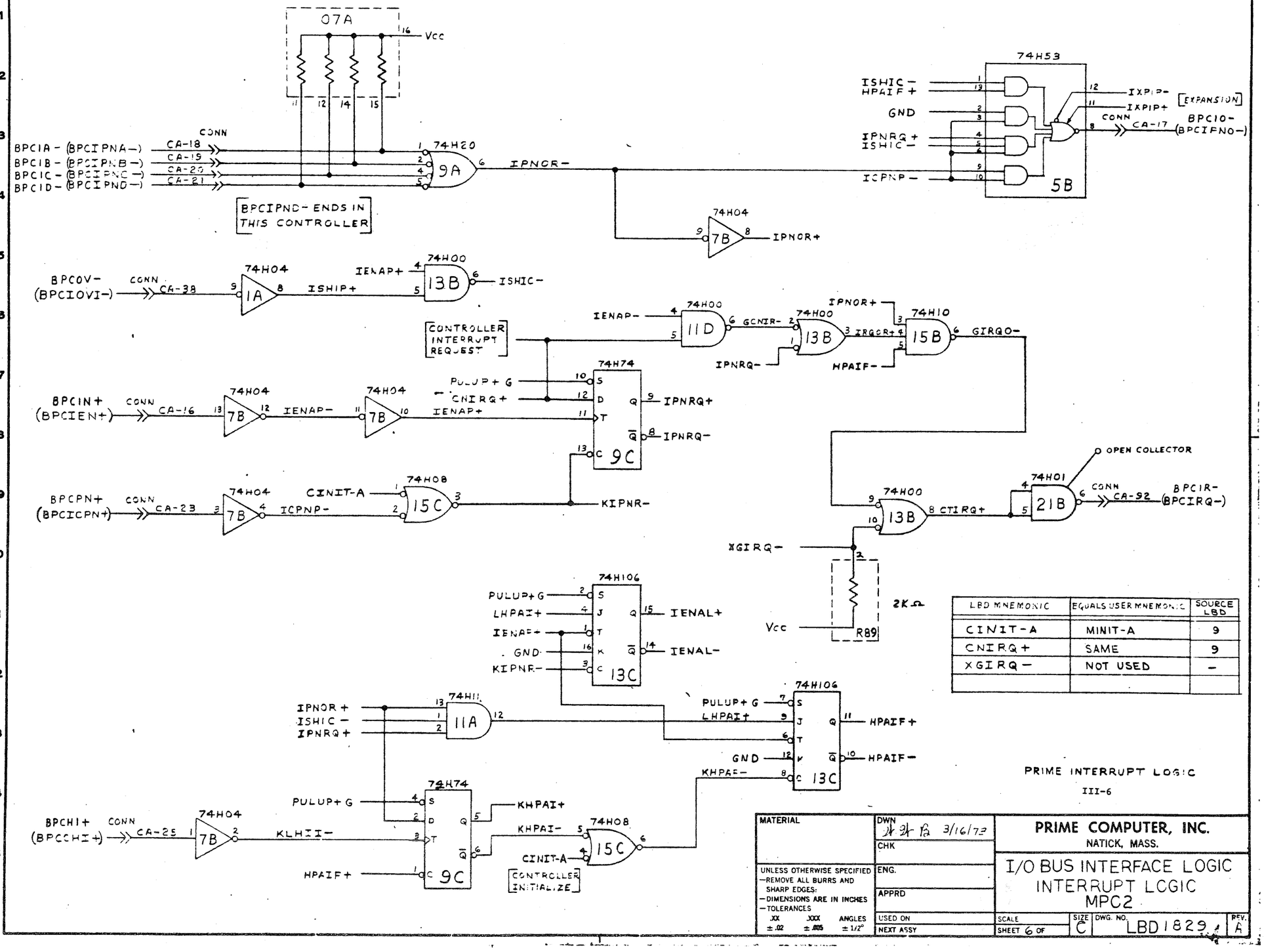


LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE PIN
DPI +	SAME	10

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	I/O BUS INTERFACE LOGIC DATA BUS LINES MPC2
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 15 OF
		SIZE C DWG. NO. LBD1829 REV A

PDF-003

PRIME COMPUTER, INC.



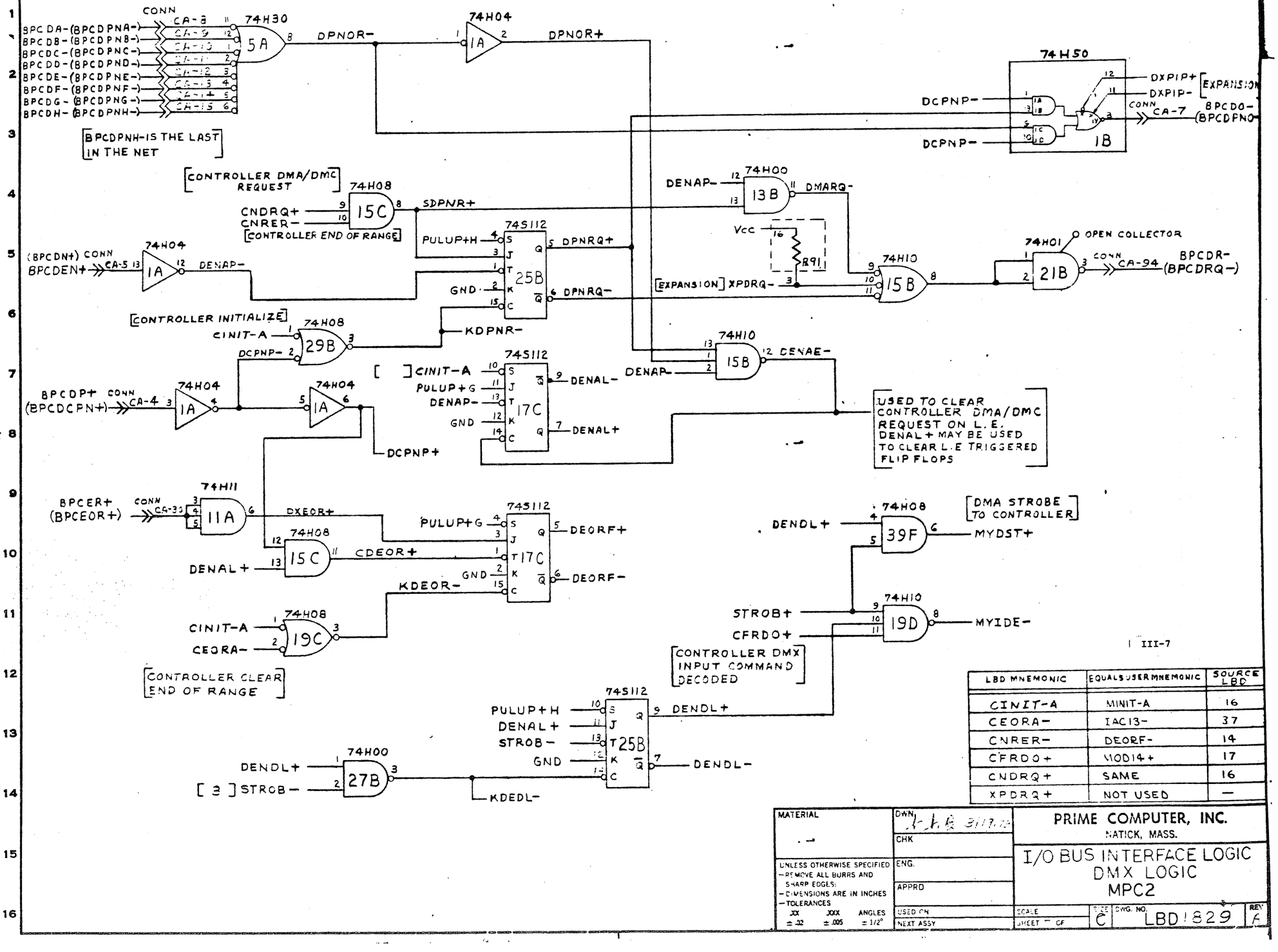
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
CINIT-A	MINIT-A	9
CNIRQ+	SAME	9
XGIRQ-	NOT USED	-

PRIME INTERRUPT LOGIC

III-6

MATERIAL	DWN 3/16/72	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	I/O BUS INTERFACE LOGIC INTERRUPT LOGIC MPC2
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 6 OF
		SIZE C / DWG. NO. LBD1829 / REV. A

PRIME COMPUTER, INC.

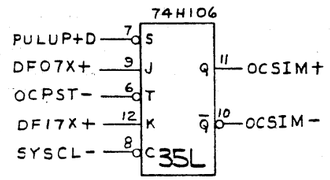


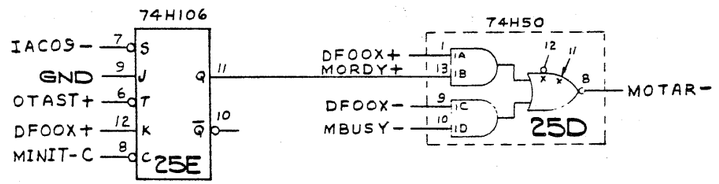
III-7

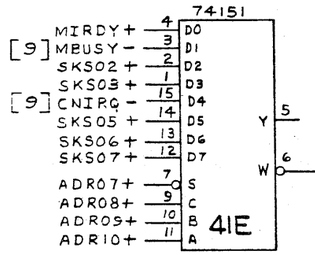
LBD MNEMONIC	EQUALS USER MNEMONIC	SOURCE LBD
CINIT-A	MINIT-A	16
CEORA-	IAC13-	37
CNRER-	DEORF-	14
CFRDO+	MIOD14+	17
CNDRQ+	SAME	16
XPDRQ+	NOT USED	—

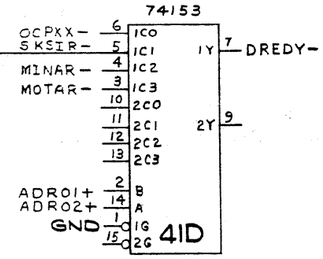
MATERIAL —	DWN	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED — REMOVE ALL BURRS AND SHARP EDGES; — DIMENSIONS ARE IN INCHES — TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	CHK	I/O BUS INTERFACE LOGIC DMX LOGIC MPC2
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET — OF
		SIZE C DWG. NO. LBD1829 REV F

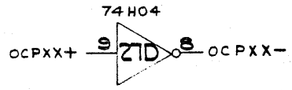
PUF-003

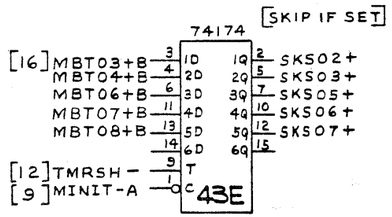


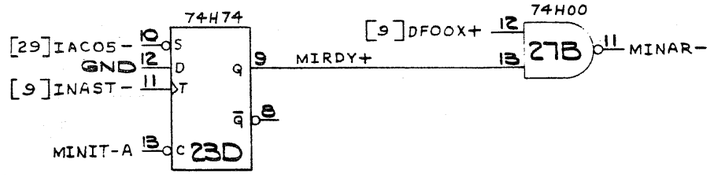


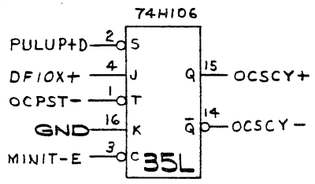












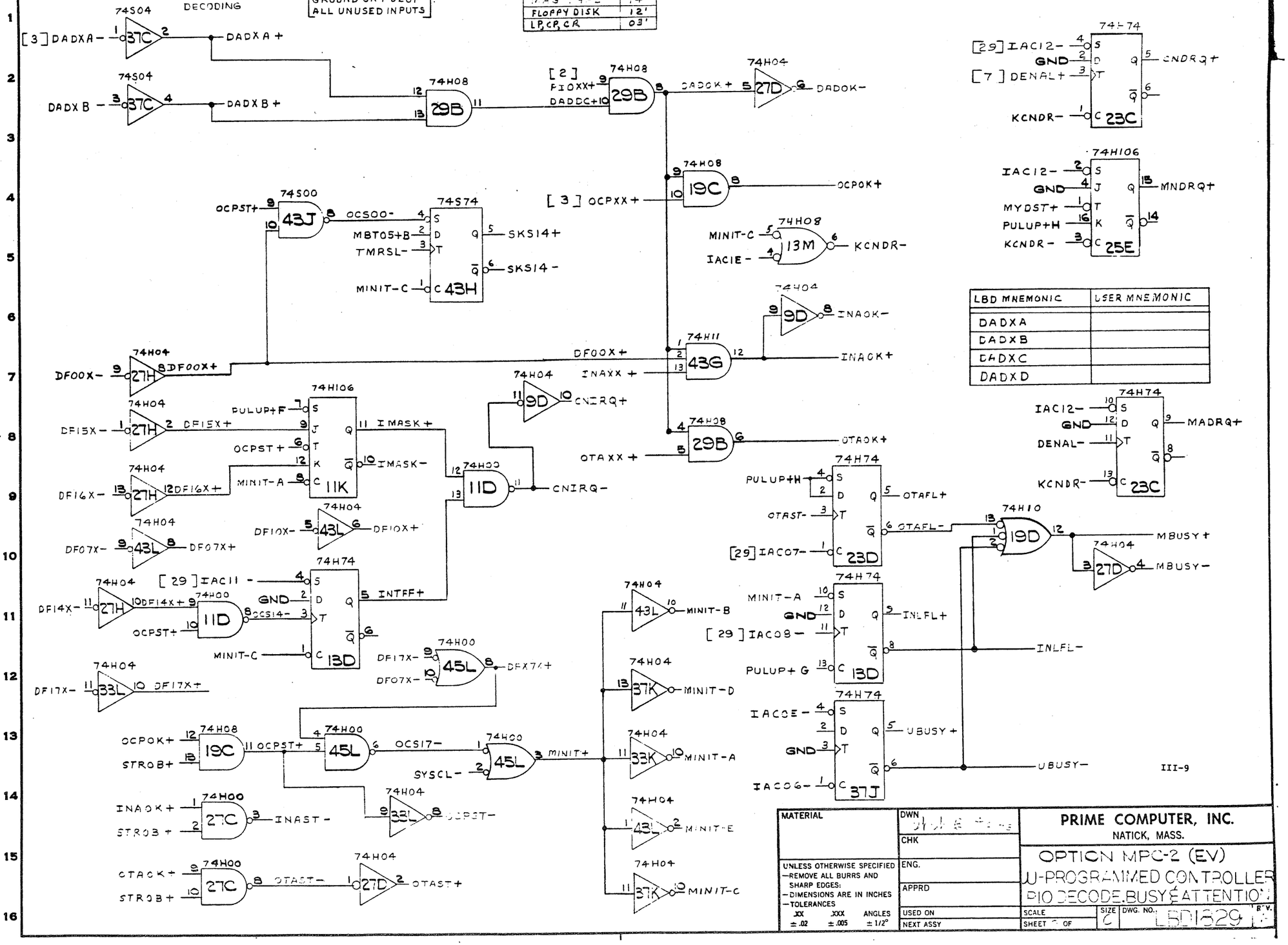
MATERIAL	DWN 12/27/73	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	OPTION MPC-2 (EV)
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	MICROPROGRAMMED CONTROLLER SKS REG & READY
	APPRD	
	USED ON	SCALE — SIZE C — DWG. NO. LBD1829 — REV. B
	NEXT ASSY	SHEET 8 OF

ADDRESS DECODING

GROUND OR PULUP ALL UNUSED INPUTS

DEVICE SELECT	
MAG TAPE	14'
FLOPPY DISK	12'
LP, CR, CR	03'

DMX REQUEST



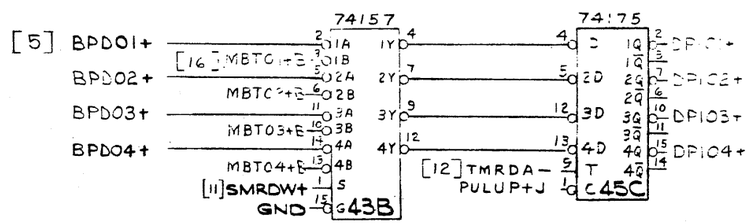
LBD MNEMONIC	USER MNEMONIC
DADXA	
DADXB	
DADXC	
DADXD	

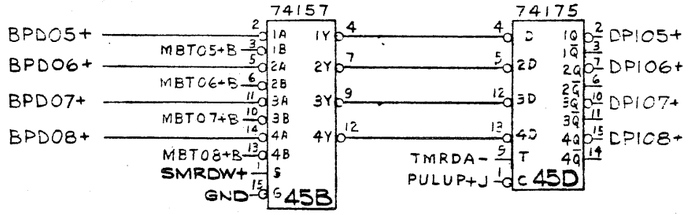
III-9

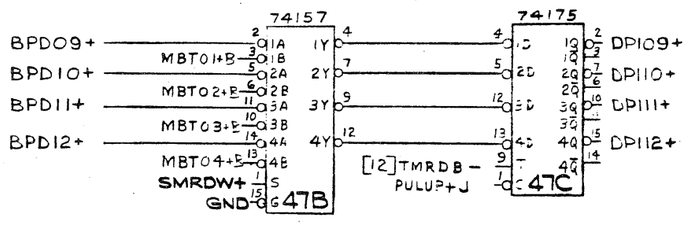
MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	OPTION MPC-2 (EV) U-PROGRAMMED CONTROLLER PIO DECODE, BUSY & ATTENTION
	ENG.	
	APPRD	
USED ON	SCALE	SIZE C DWG. NO. LBD1629 REV.
NEXT ASSY	SHEET OF	

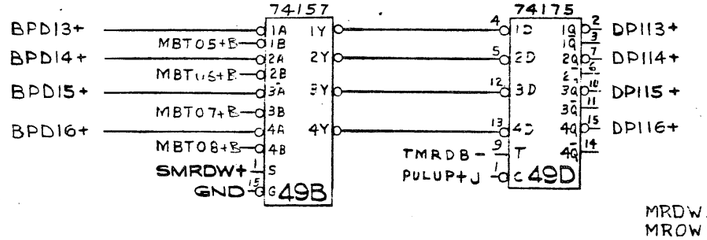
PDF-003

DATA REG

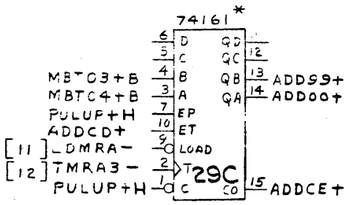


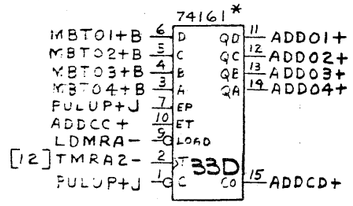


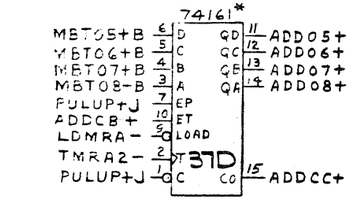


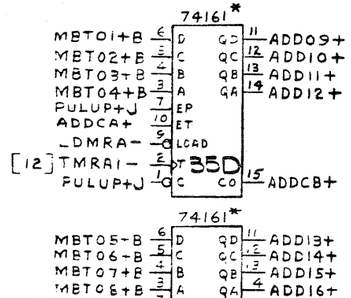


TE

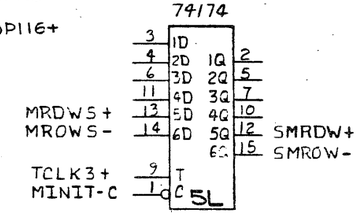


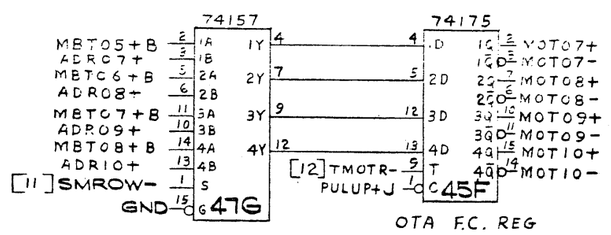




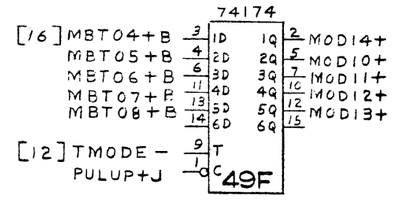


ADDRESS REGISTER

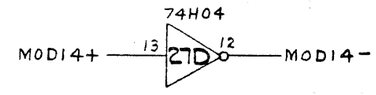


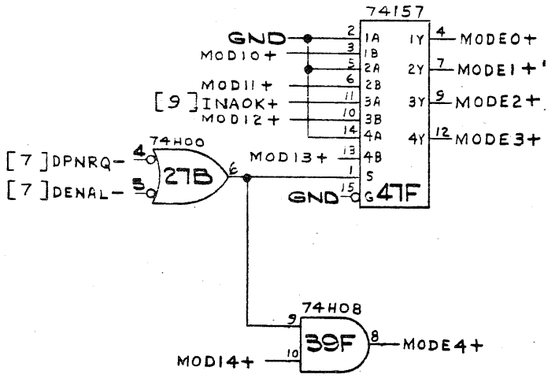


OTA F.C. REG



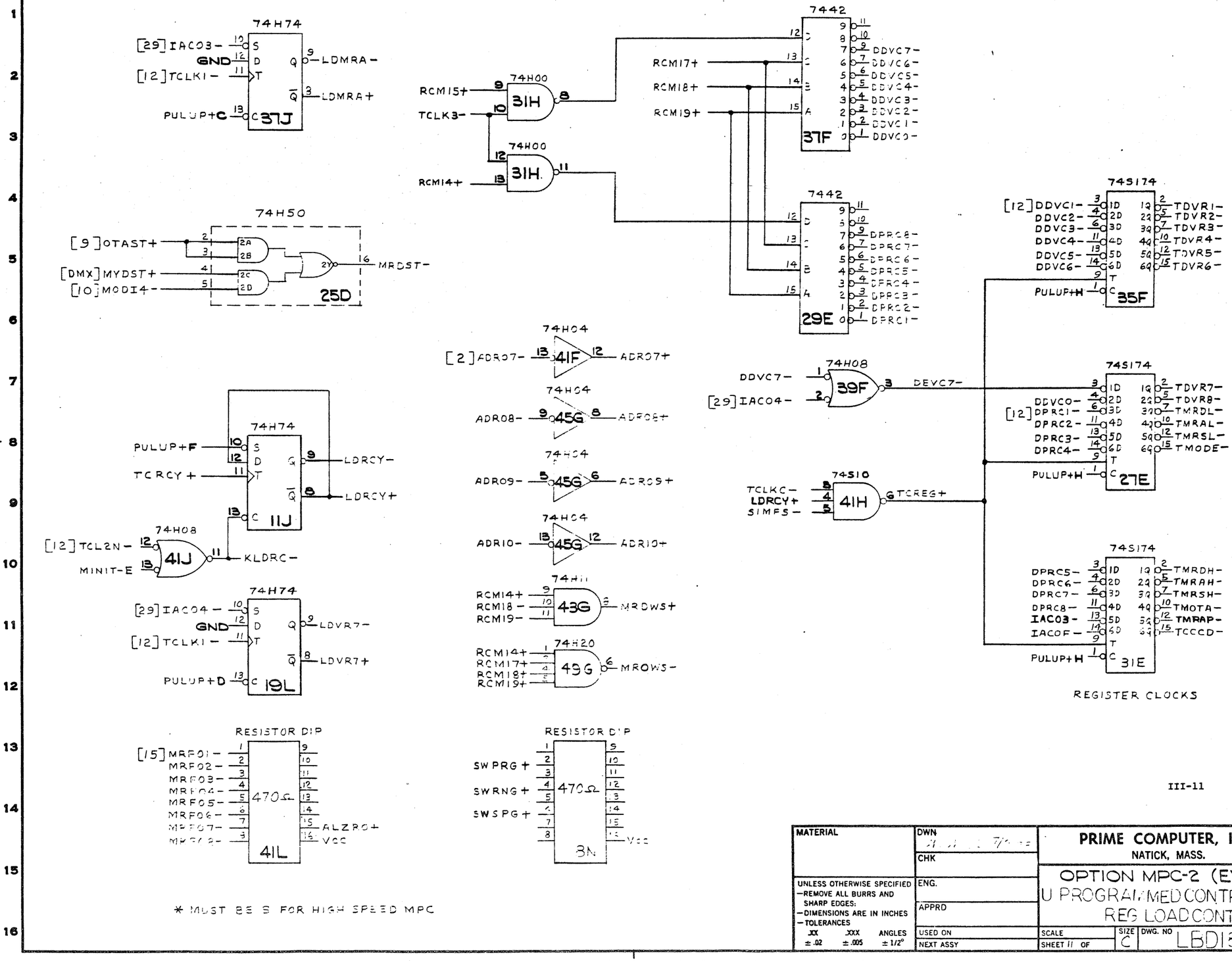
MODE LINE REGISTER





*NEED S IN HIGH SPEED MPC

MATERIAL	DWN 3/26/73	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED: -REMOVE ALL BURRS AND SHARP EDGES; -DIMENSIONS ARE IN INCHES -TOLERANCE: .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	OPTION MPC-2 (EV) PROGRAMMED CONTROLLER ADDRESS & DATA REGISTEPS	
	ENG		
	APPRD		
	MFG	SCALE	SIZE C DWG NO LBD1829 REV A
	NEXT ASSY	SHEET 10 OF	



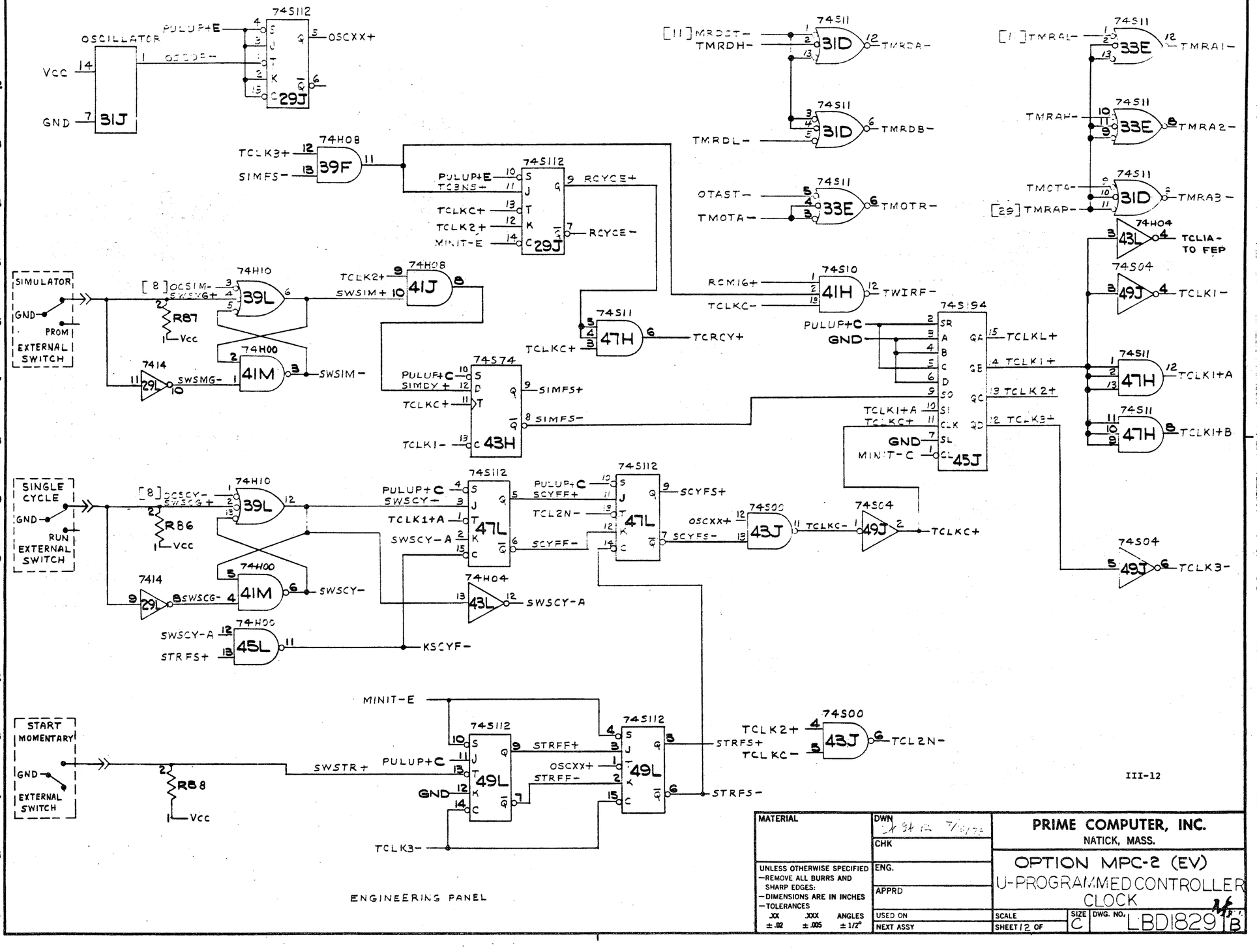
REGISTER CLOCKS

* MUST BE S FOR HIGH SPEED MPC

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	OPTION MPC-2 (EV) U PROGRAMMED CONTROLLER REG LOAD CONTROLS	
	APPRD		
	USED ON	SCALE	SIZE C DWG. NO LBD1829 REV -
	NEXT ASSY	SHEET 11 OF	

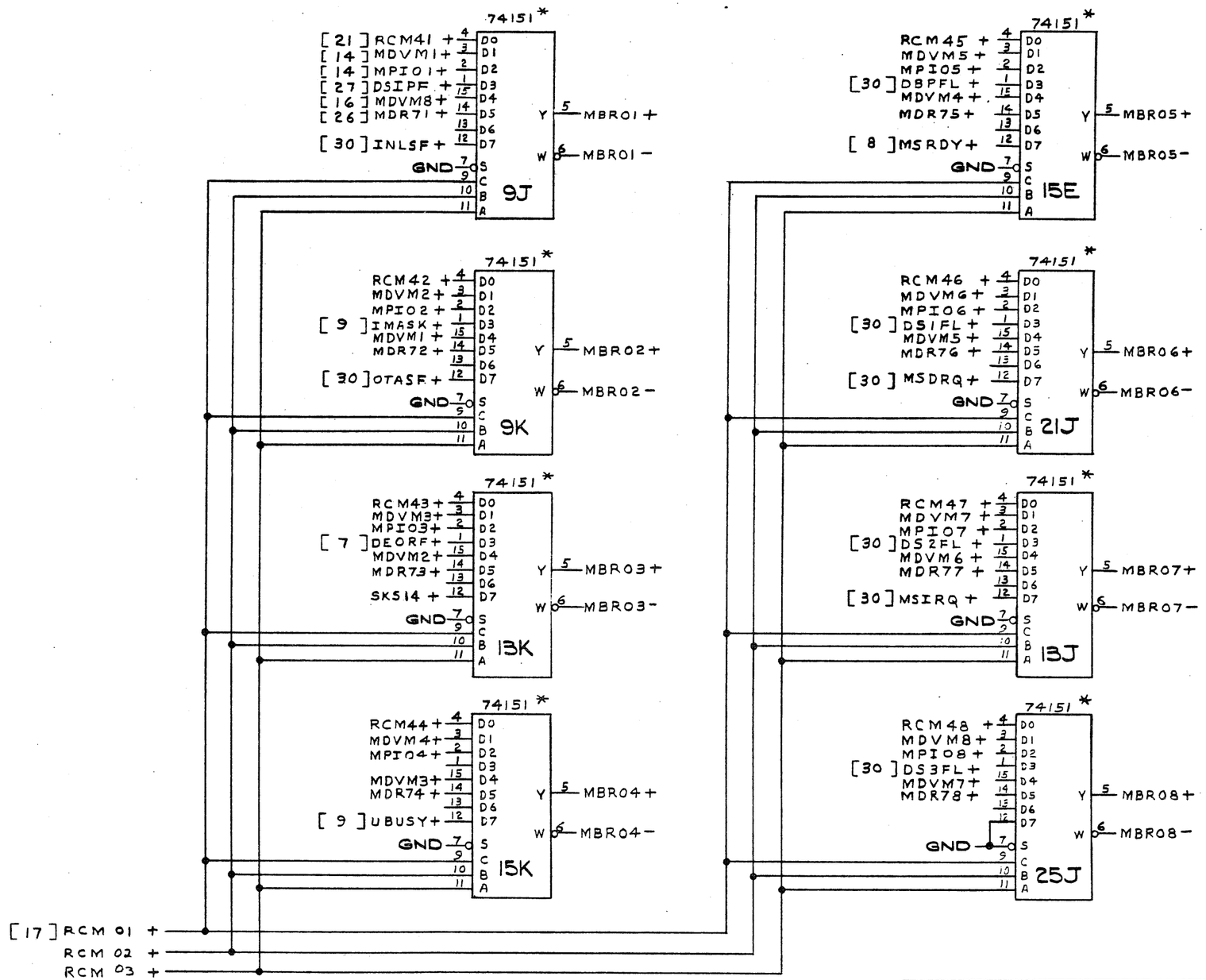
PDF-003

PRIME COMPUTER, INC.



III-12

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	OPTION MPC-2 (EV) U-PROGRAMMED CONTROLLER CLOCK
	ENG.	
	APPRD	
USED ON	SCALE	SIZE C DWG. NO. LBD1829 B
NEXT ASSY	SHEET 12 OF	

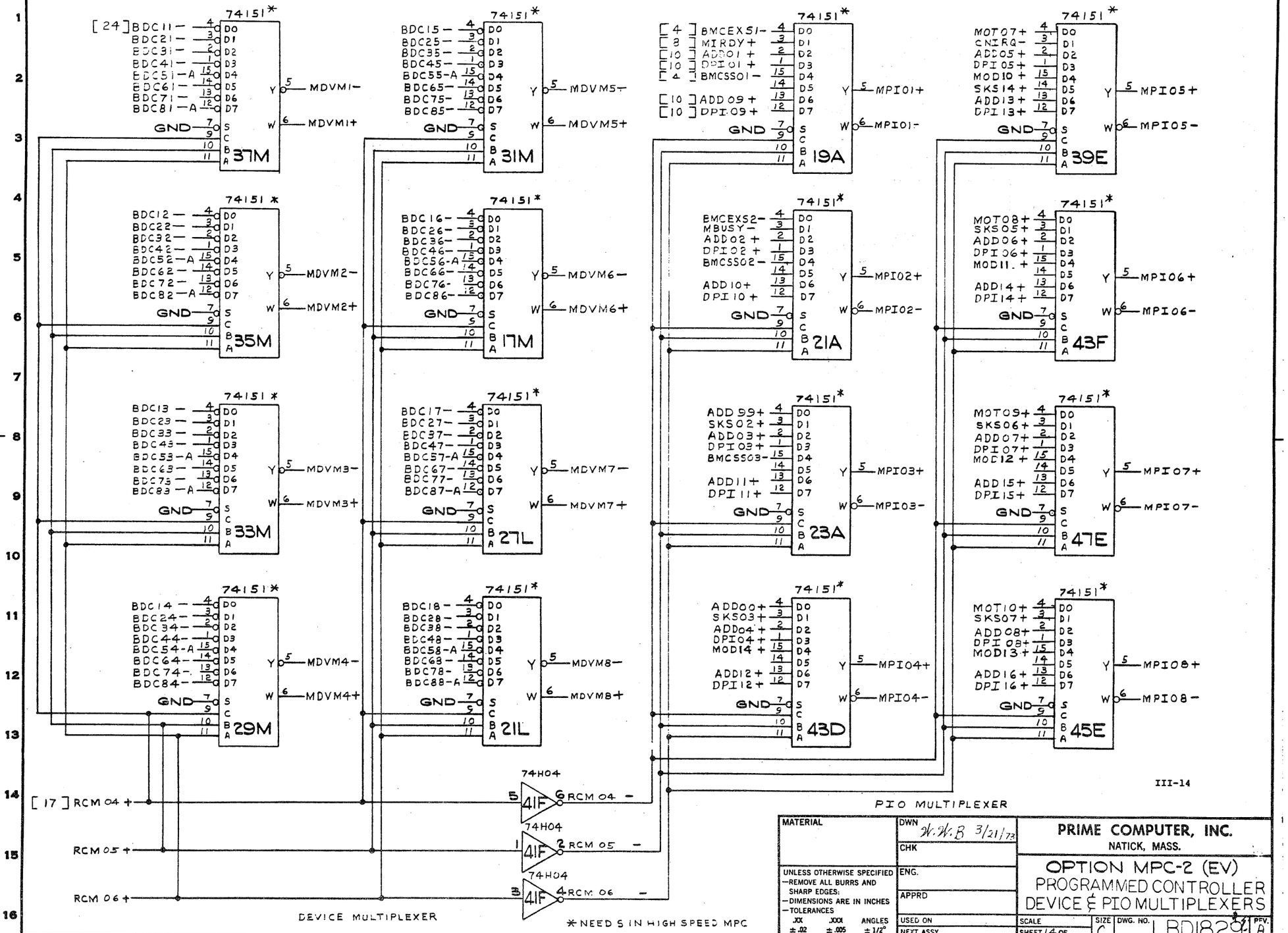


* NEED S IN HIGH SPEED MPC

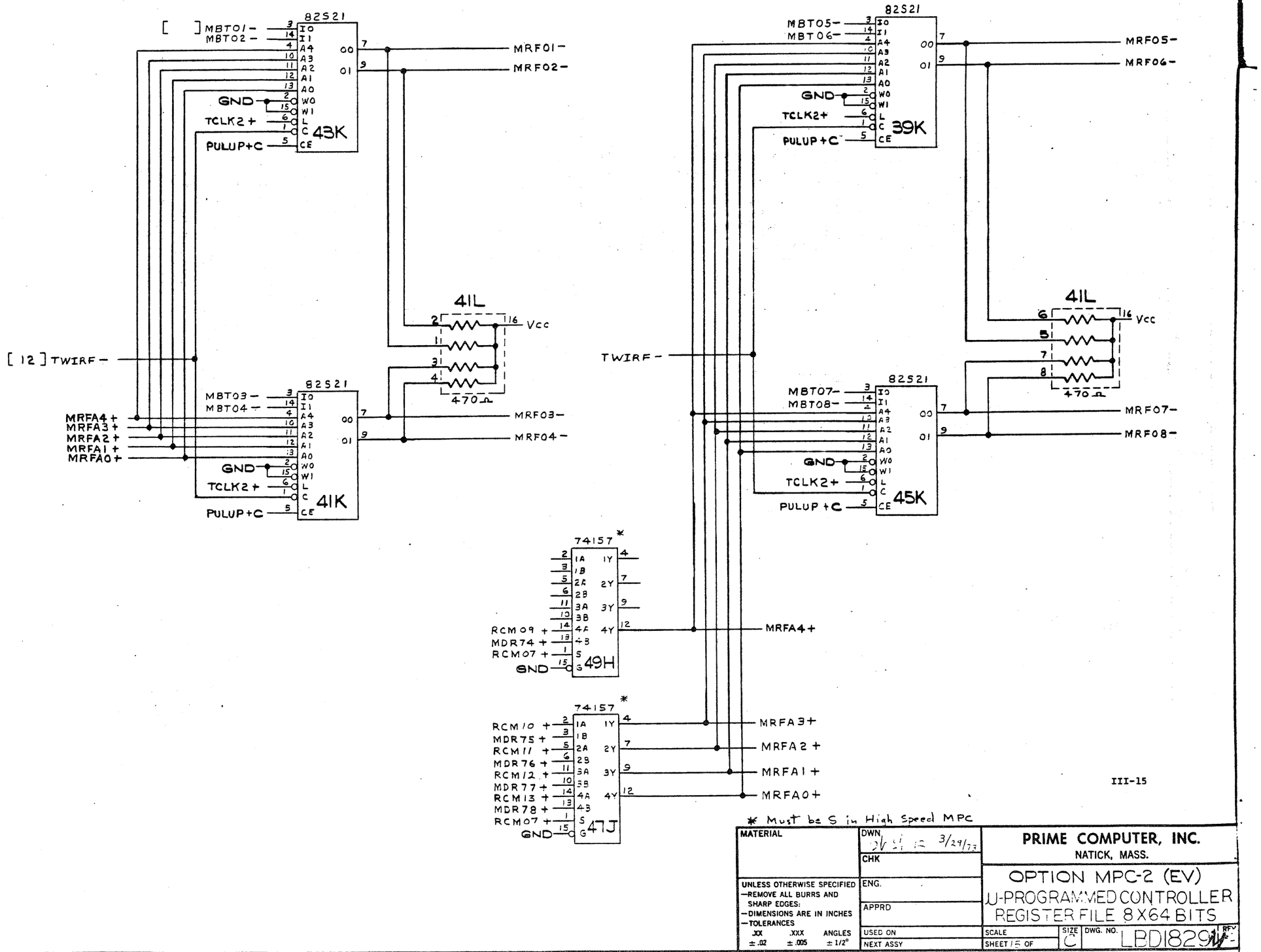
MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	OPTION MPC-2 (EV) U-PROGRAMMED CONTROLLER RECEIVE BUS MULTIPLEXER
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 3 OF
		SIZE C / DWG. NO. LBD1829 / REV. M

PDF-003

PRIME COMPUTER, INC.



MATERIAL	DWN W.W.B 3/21/73	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	OPTION MPC-2 (EV) PROGRAMMED CONTROLLER DEVICE & PIO MULTIPLEXERS
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 14 OF / SIZE C / DWG. NO. LBD1829 / REV. A



III-15

MATERIAL	DWN. 3/29/73	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES: –DIMENSIONS ARE IN INCHES –TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	OPTION MPC-2 (EV) U-PROGRAMMED CONTROLLER REGISTER FILE 8X64 BITS
	APPRD	
	USED ON	SCALE / SIZE C / DWG. NO. LBD1829 / REV
	NEXT ASSY	SHEET 15 OF

PDF-003

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

Arithmetic Unit — Bit Test — Transmit Bus

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

74181 * 23K

[13] MBR01- MBR02- MBR03- MBR04-

[15] MRF01- MRF02- MRF03- MRF04-

[19] RCM22-

RCM23-

RCM24-

RCM25-

ALCO5+

F3 F2 F1 F0 → MBT01- MBT02- MBT03- MBT04-

A=B → ALZRO+

CN+4 → ALCO1+

P G

74151 * 23J

D0 D1 D2 D3 D4 D5 D6 D7 S C B A

GND RCM34+ RCM35+ RCM36+

Y → BBIT1-

W → BBIT1+

74181 * 19K

MBR05- MBR06- MBR07- MBR08-

MRF05- MRF06- MRF07- MRF08-

F3 F2 F1 F0 → MBT05- MBT06- MBT07- MBT08-

A=B → ALZRO+

CN+4 → ALCO5+

ALCO9-

74H04 * 27J → ALZRO-

R02 470Ω Vcc

74H08 * 41J

RCM20+ RCM21+ → ALOGC+

MBT08-

74H04 * 41F MBT01+A

74H04 * 41F MBT01+B

74H04 * 33K MBT02+A

74H04 * 47K MBT02+B

74H04 * 47K MBT03+A

74H04 * 41F MBT03+B

74H04 * 33L MBT04+A

74H04 * 27J MBT04+B

74H04 * 33K MBT05+A

74H04 * 37K MBT05+B

74H04 * 33K MBT06+A

74H04 * 37K MBT06+B

74H04 * 47K MBT07+A

74H04 * 45G MBT07+B

74H04 * 47K MBT08+A

74H04 * 47K MBT08+B

74194 * 21E

SR A B C D SO SI CLK SL CL

ALCO1+ MBT01- ALZRO- BBIT1+ [29] PULUP+H [11] TCCCD- MINIT-C

QA → 15 CCCRY+

QB → 14 CCMNS-

QC → 13 CCZERO-

QD → 12 CCBIT+

74H04 * 9D → CCBIT-

74H00 * 31H RCM20+ RCM21- ALCIN- → ALCO9+

74H00 * 23H → ALLEZ+

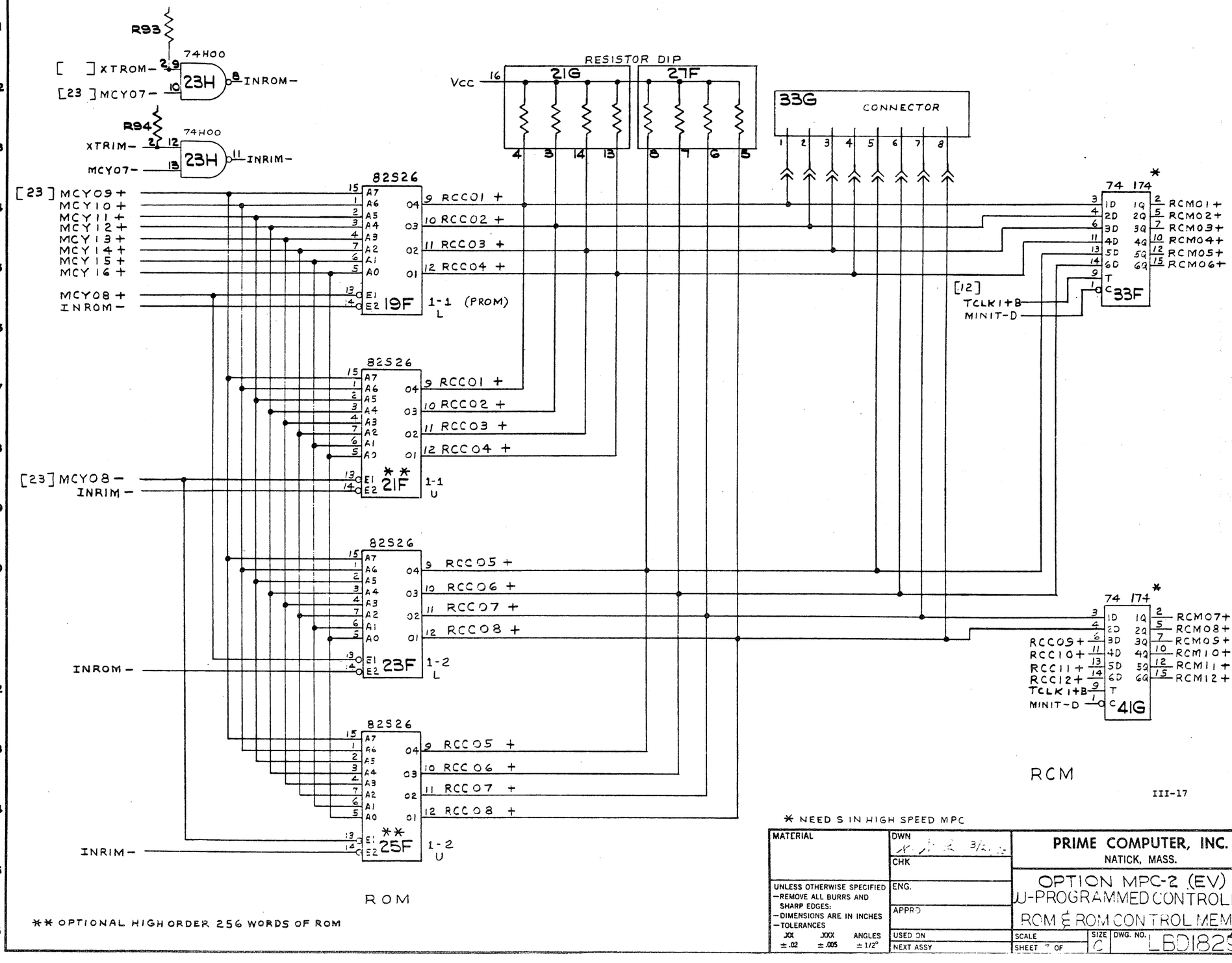
74H04 * 9D → CCMNS+

74H04 * 9D → CCZERO+

III-16

* Need to be S in High Speed MPC

MATERIAL	DWN W.W.L. 3/28/75	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK	OPTION MPC-2 (EV) MU-PROGRAMMED CONTROLLER ALU, BIT TEST AND BT	
	ENG.		
	APPRD		
USED ON / NEXT ASSY	SCALE / SHEET 16 OF	SIZE C	DWG. NO. LBD1829 REV. A



MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES; –DIMENSIONS ARE IN INCHES –TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	OPTION MPC-2 (EV) U-PROGRAMMED CONTROLLER ROM & ROM CONTROL MEMORY
	APPR'D	
	USED ON	SCALE / SIZE C / DWG. NO. LBD1829 / REV. L
	NEXT ASSY	SHEET 7 OF

PDF-003

PRIME COMPUTER, INC.

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

PULUP+G 16
GND 15
PULUP+E 14
MCY08+ 10
GND 9
MCY07+ 11
XTROM- 12
XTRIM- 13

25H CONNECTOR

1 2 3 4 5 6 7 9

PESISTOR DIP

Vcc 16 — 27F — 21G — 16 Vcc

9 10 11 12 — 8 7 6 5

33G CONNECTOR

9 10 11 12 13 14 15 16

[23] MCY09+
MCY10+
MCY11+
MCY12+
MCY13+
MCY14+
MCY15+
MCY16+
MCY08+
INROM-

82S26 — 29F — 2-1 L

A7 A6 A5 A4 A3 A2 A1 A0 — E1 E2 — O4 O3 O2 O1

9 RCC09+
10 RCC10+
11 RCC11+
12 RCC12+

82S26 — 31F — 2-1 U **

MCY08-
INRIM-

9 RCC09+
10 RCC10+
11 RCC11+
12 RCC12+

82S26 — 19G — 2-2 L

INROM-

9 RCC13+
10 RCC14+
11 RCC15+
12 RCC16+

82S26 — 17G — 2-2 U **

INRIM-

9 RCC13+
10 RCC14+
11 RCC15+
12 RCC16+

74H04 *

RCM18+ — 1 — 45G — 2 — RCM18-

74 174 *

RCC17+ 13
RCC18+ 14
[12] TCLK1+B 9
MINIT-D 1

3D 4D 5D 6D — T C — 39G

1Q 2Q 3Q 4Q 5Q 6Q

2 RCM13+
5 RCM14+
7 RCM15+
10 RCM16+
12 RCM17+
15 RCM18+

ROM

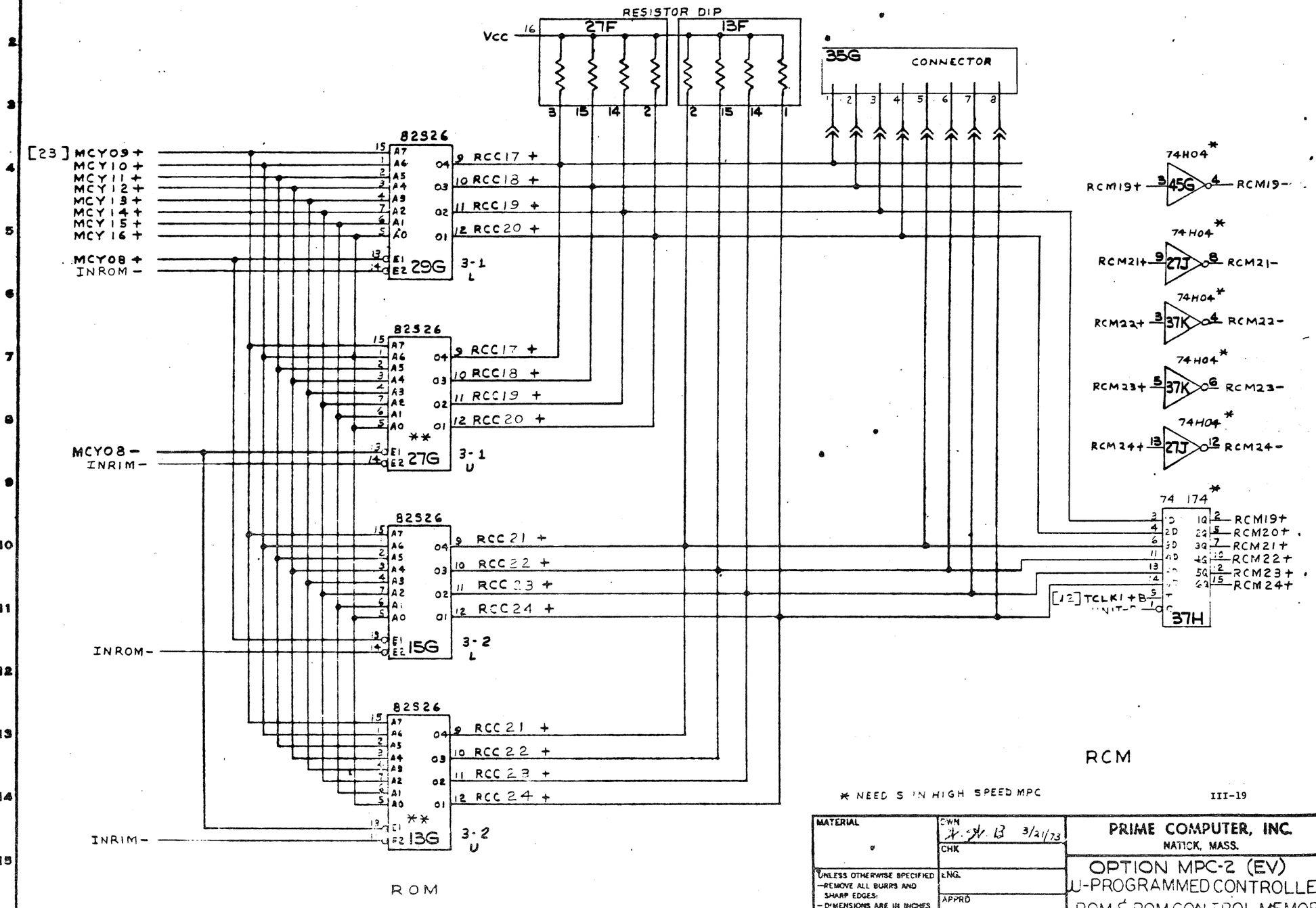
** OPTIONAL HIGH ORDER 256 WORDS OF ROM

RCM

III-18

* NEED S IN HIGH SPEED MPC

MATERIAL	DWN 3/21/75	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	OPTION MPC-2 (EV)
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	U-PROGRAMMED CONTROLLER
	APPRD	ROM & ROM CONTROL MEMORY
USED ON	SCALE	SIZE C DWG. NO LBD1829 REV A
NEXT ASSY	SHEET 8 OF	

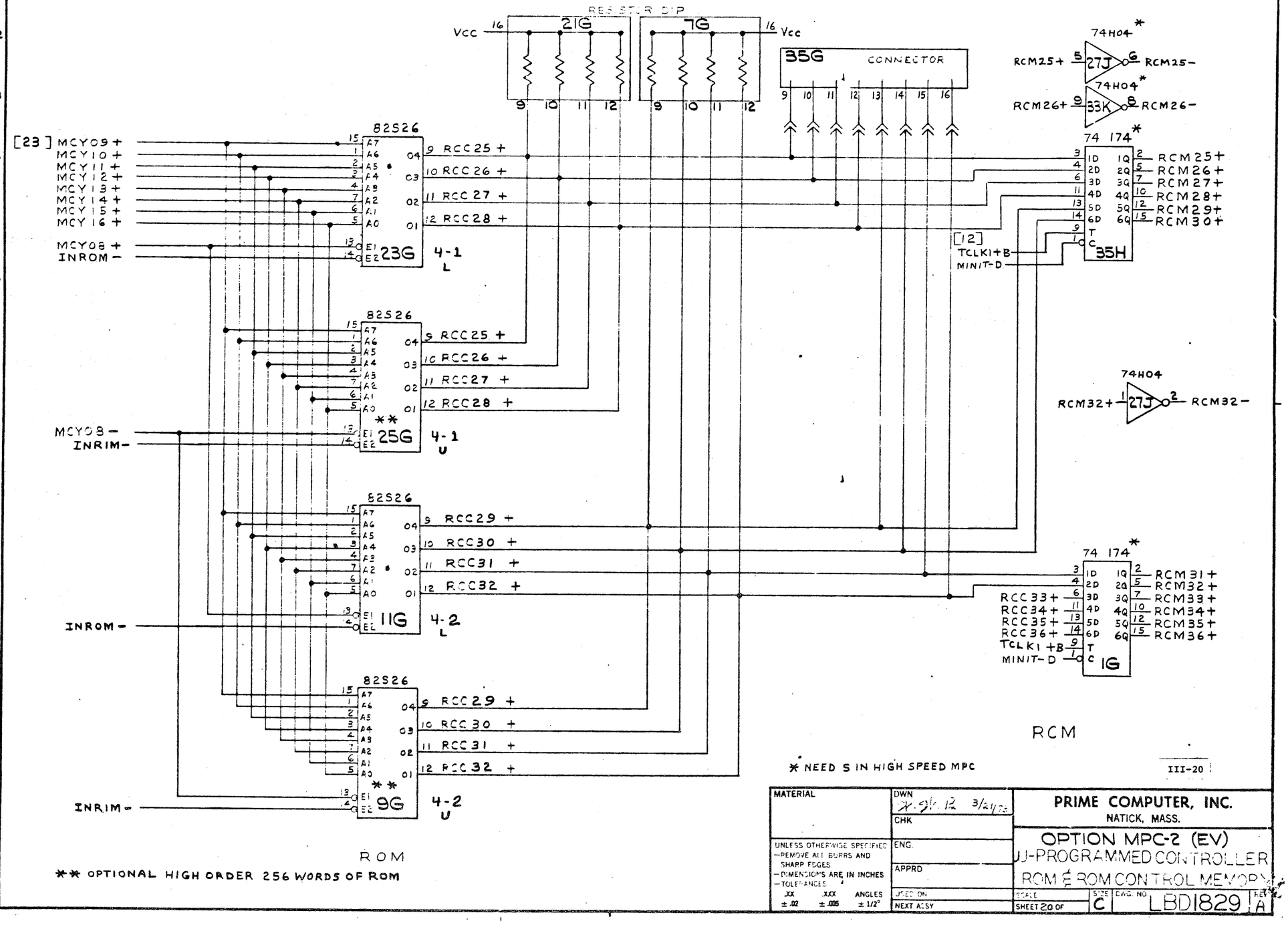


III-19

MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: — DIMENSIONS ARE IN INCHES — TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	CHK	OPTION MPC-2 (EV) U-PROGRAMMED CONTROLLER ROM & ROM CONTROL MEMORY
	ENG.	
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 1 OF
		SIZE C — DWG. NO LBD1829 — REV E

P05-005

PRIME COMPUTER, INC.



ROM

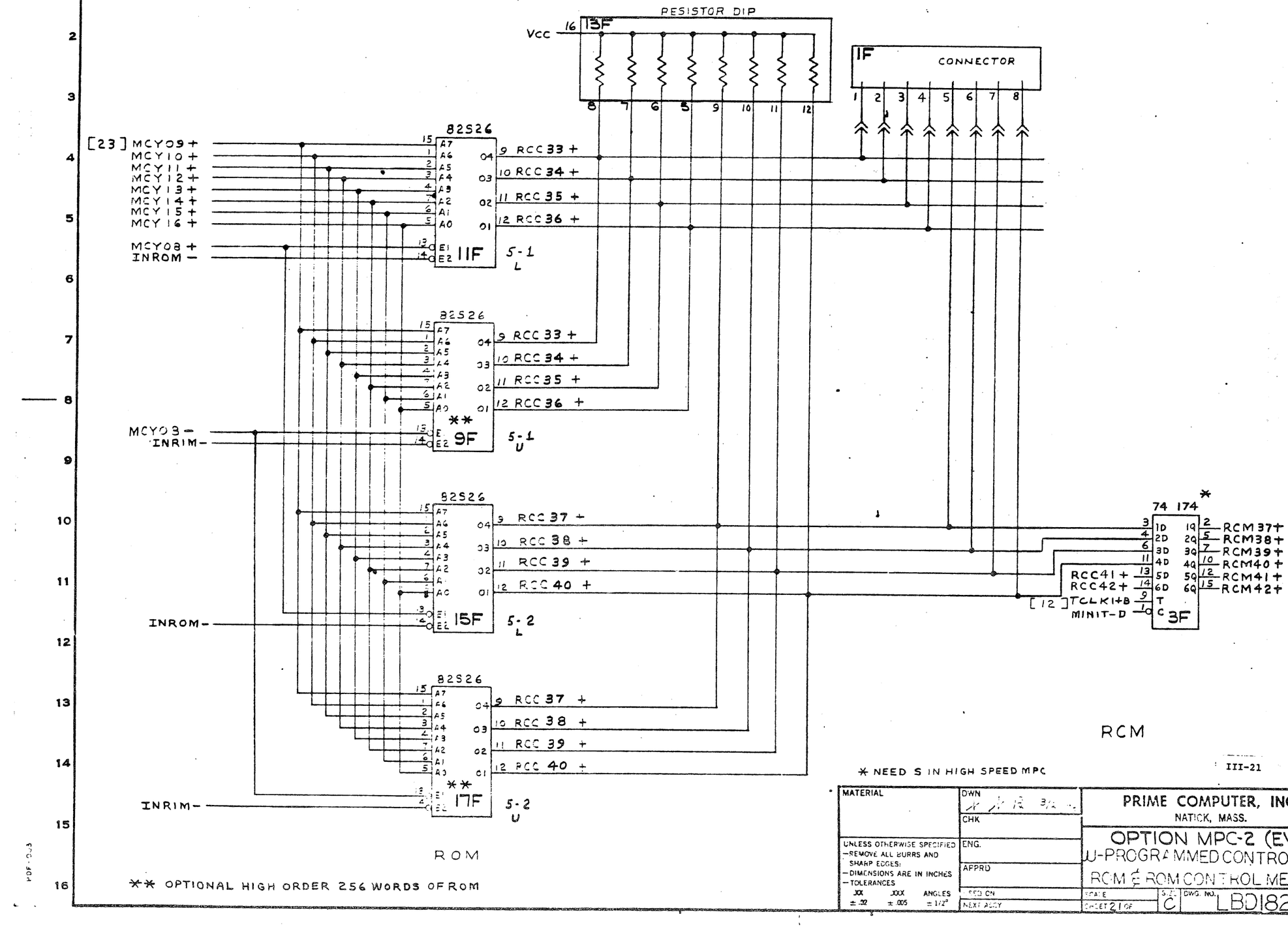
** OPTIONAL HIGH ORDER 256 WORDS OF ROM

RCM

* NEED S IN HIGH SPEED MPC

MATERIAL	DWN K.G.K. 12 3/21/75	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	OPTION MPC-2 (EV) MU-PROGRAMMED CONTROLLER ROM & ROM CONTROL MEMORY
	APPRD	
	USED ON NEXT ASSY	SCALE SHEET 20 OF
		SIZE C DWG. NO. LBD1829 REV A

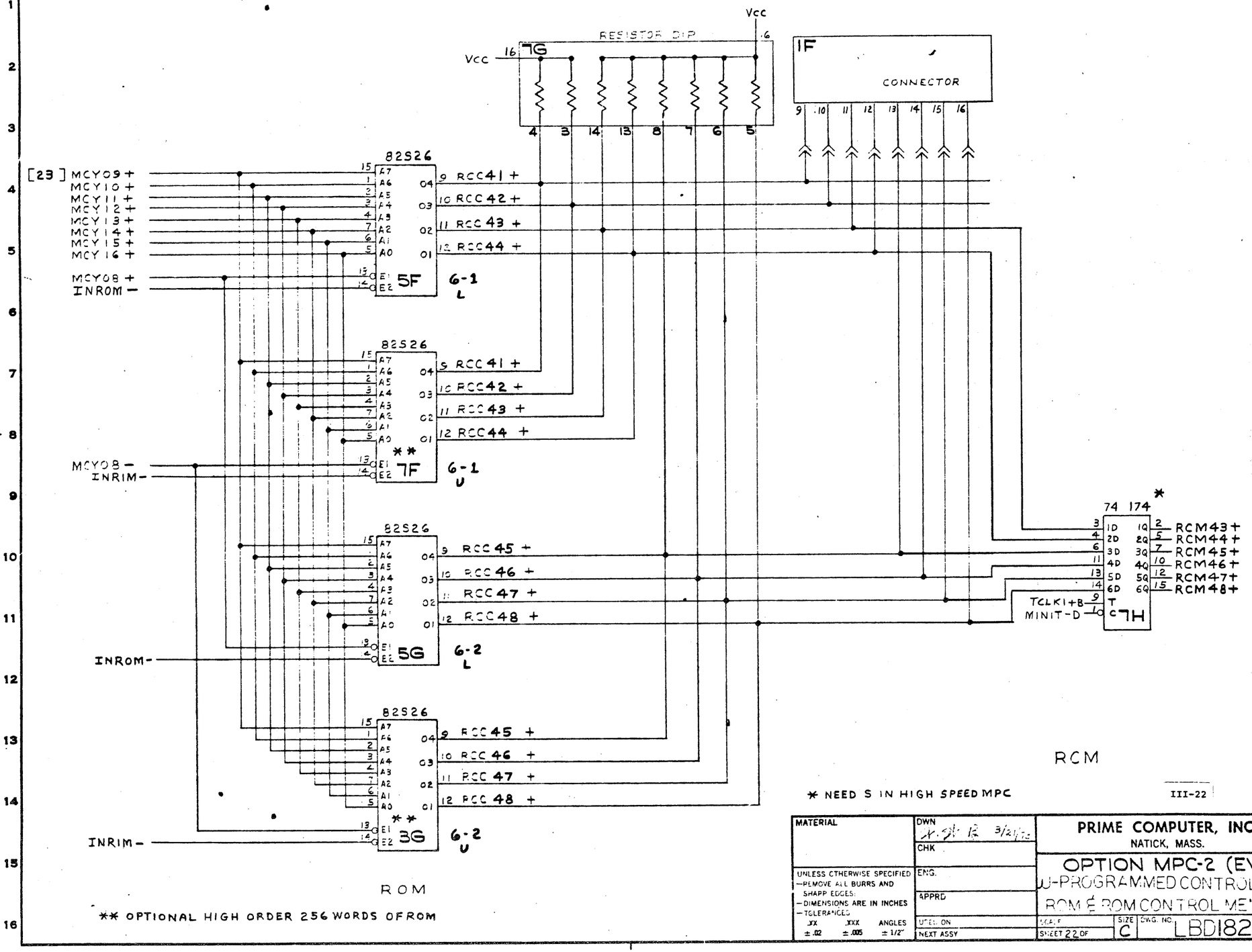
PRIME COMPUTER, INC.



III-21

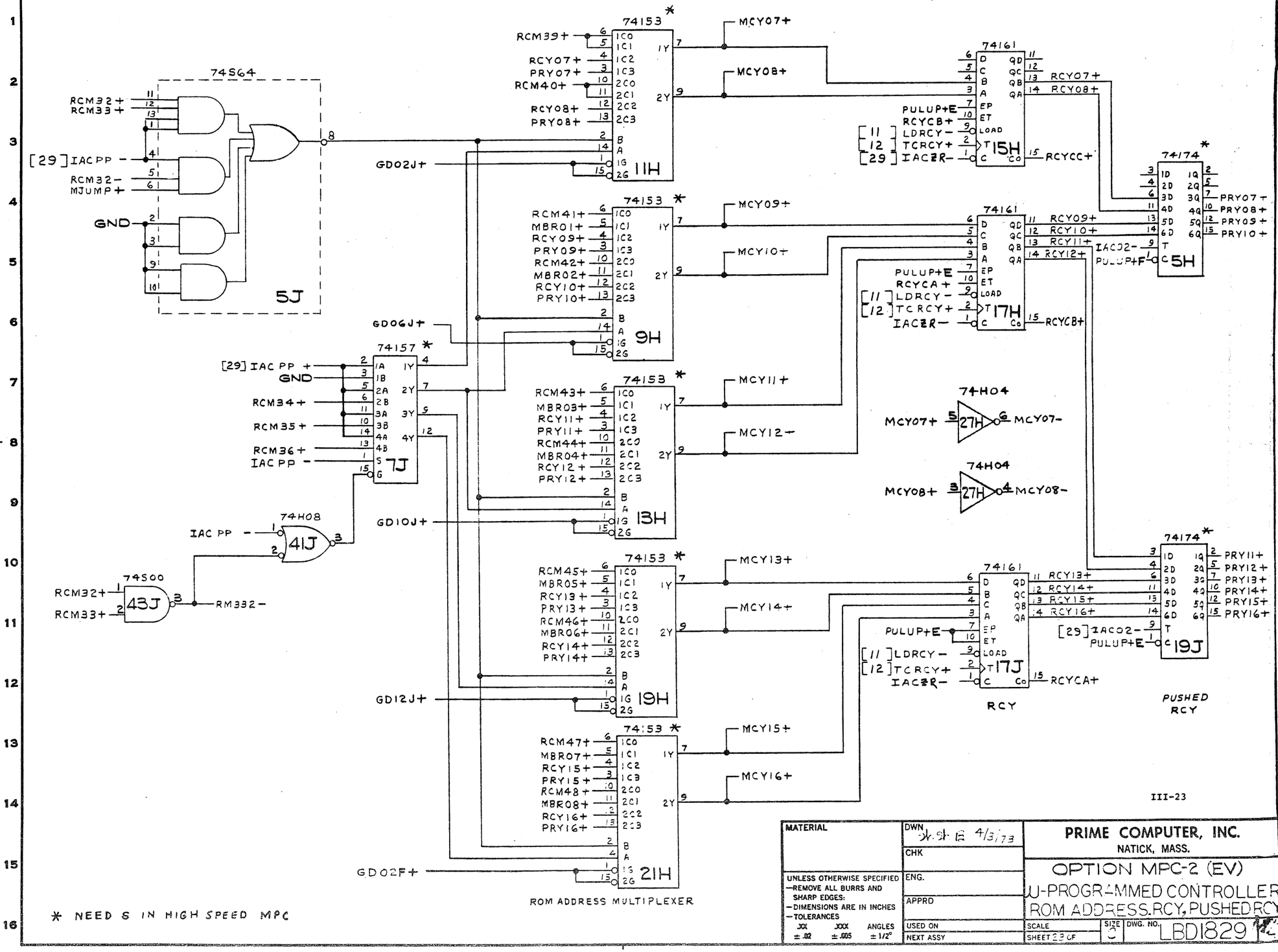
MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED –REMOVE ALL BURRS AND SHARP EDGES: –DIMENSIONS ARE IN INCHES –TOLERANCES XX ±.02 XXX ±.005 ANGLES ±1/2°	ENG.	OPTION MPC-2 (EV) U-PROGRAMMED CONTROLLER
	APPRD	ROM & ROM CONTROL MEMORY
	NEXT ASSY	SCALE SHEET 21 OF SIZE C DWG. NO. LBD1829 REV A

PRIME COMPUTER, INC.



III-22

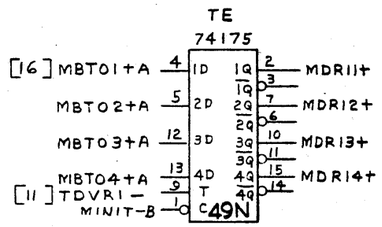
MATERIAL	DWN N. St. 12 3/21/75	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	OPTION MPC-2 (EV) U-PROGRAMMED CONTROLLER ROM & PROM CONTROL MEMORY
	APPRD	
	USED ON NEXT ASSY	SCALE SHEET 22 OF
		SIZE C DWG. NO. LBD1829 REV. A

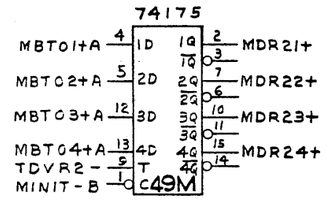


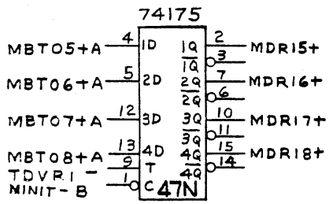
III-23

MATERIAL	DWN W.St 12 4/3/73	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	OPTION MPC-2 (EV)
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	U-PROGRAMMED CONTROLLER ROM ADDRESS.RCY, PUSHED RCY
	APPRD	
USED ON	SCALE	SIZE C DWG. NO. LBD1829
NEXT ASSY	SHEET 23 OF	

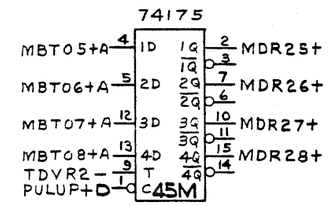
PDF-003







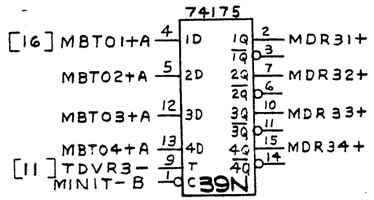
DEVICE REGISTER 1

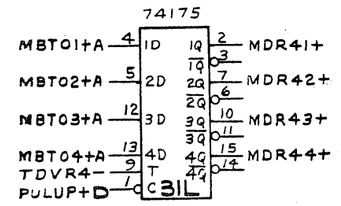


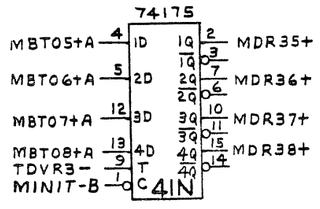
DEVICE REGISTER 2

* NEED S IN HIGH SPEED MPC

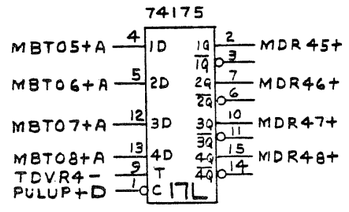
MATERIAL	DWN. W.W. 12 7/11/73	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	OPTION MPC-2 (EV)
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	U-PROGRAMMED CONTROLLER
	APPRD	DEVICE REGISTERS 1 AND 2
USED ON / NEXT ASSY	SCALE / SHEET 24 OF	SIZE C / DWG. NO. LBD1829 / REV. A



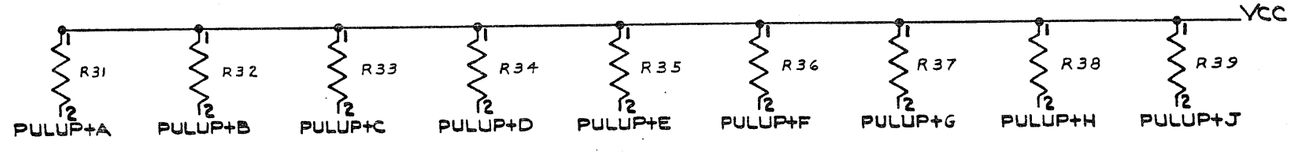




DEVICE REGISTER 3



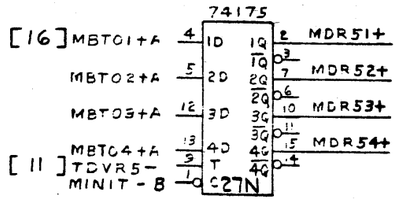
DEVICE REGISTER 4

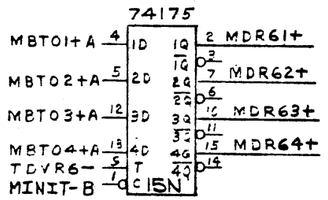


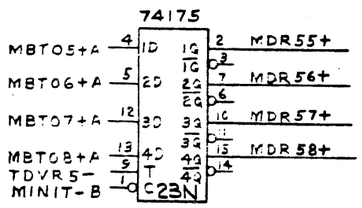
* NEED S IN HIGHSPEED MPC

MATERIAL	DWN 3K - 6 74175	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	OPTION MPC-2 (EV) U-PROGRAMMED CONTROLLER DEVICE REGISTERS 3 AND 4
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 25 OF	SIZE C	DWG. NO. LED1829	REV. 4

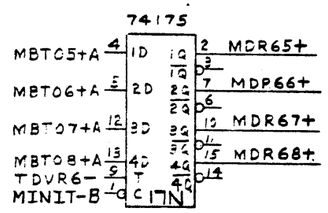
PDF-003



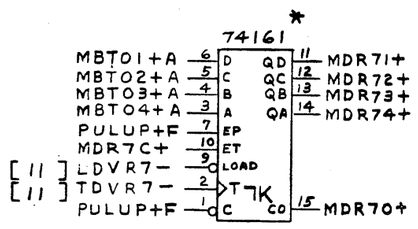


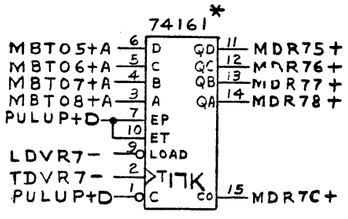


DEVICE REGISTER 5



DEVICE REGISTER 6

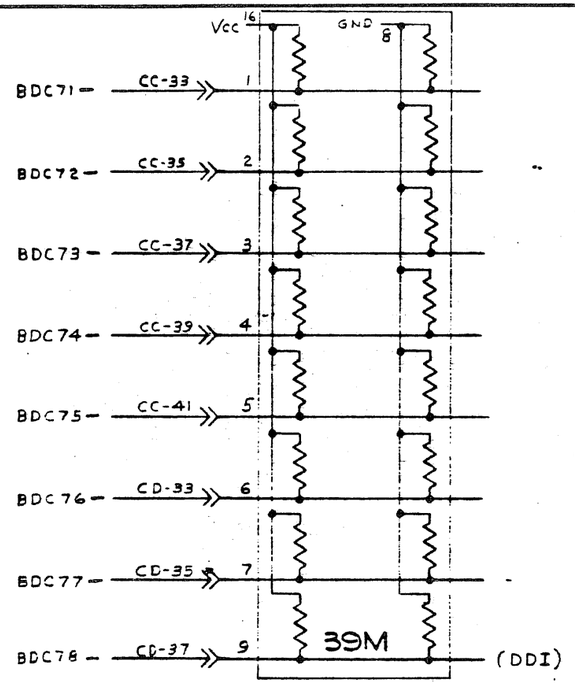


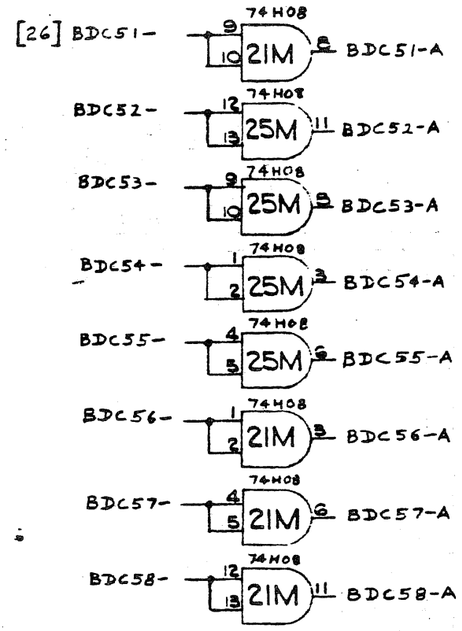


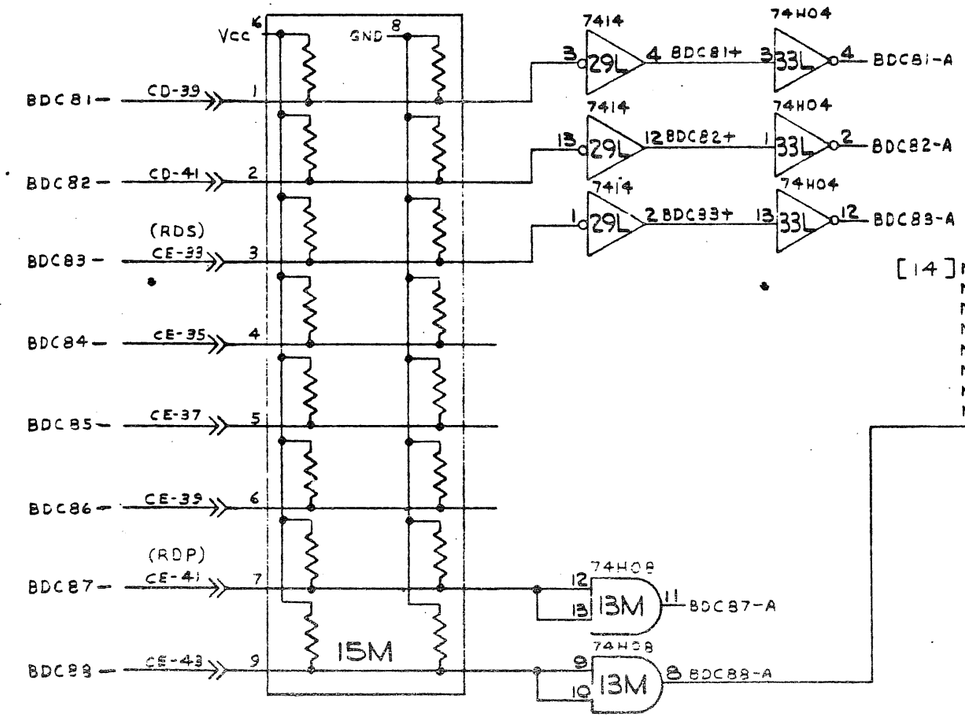
DEVICE REGISTER 7

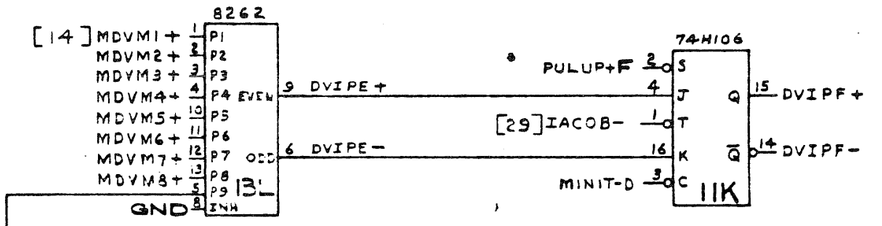
* NEED S IN HIGH SPEED MPC

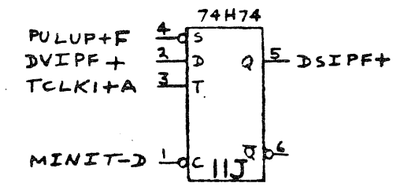
MATERIAL	DWN M.H. 3/23/73	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	OPTION MPC-2 (EV) U-PROGRAMMED CONTROLLER DEVICE REGISTERS 5 THRU 7	
	APPRD		
	USED ON / NEXT ASSY	SCALE / SHEET 26 OF	SIZE C / DWG. NO. LBD1829 / REV. A









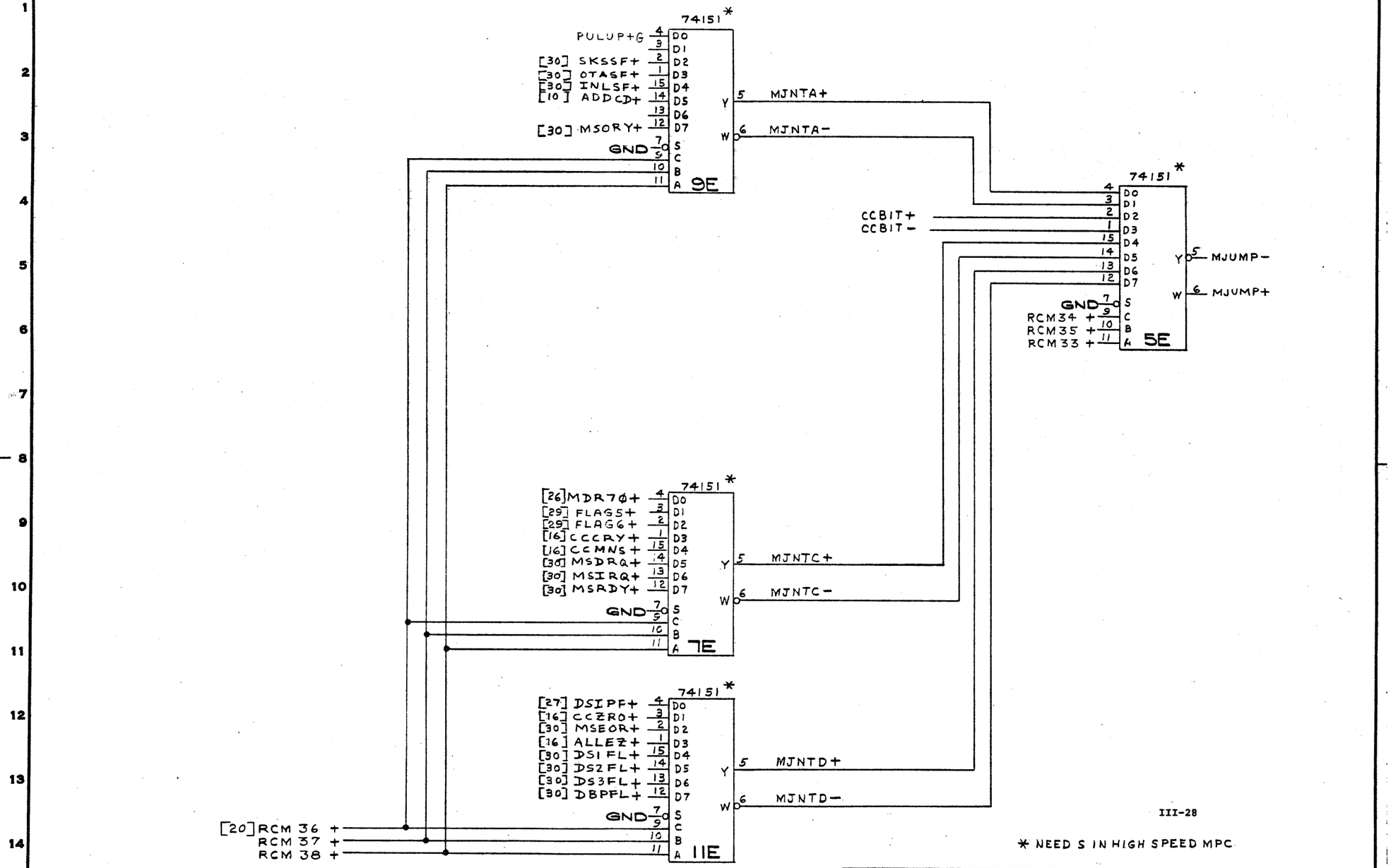


III-27

MATERIAL	DWN H. H. B 3/22/74	PRIME COMPUTER, INC. NATICK, MASS.	
	CHK		
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES; —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	MAG TAPE READ & CONTRO U-PROGRAMMED CONTROLLER DEVICE BUS INPUT & PARITY	
	APPRD 4-9-74		
	NEXT ASSY	SHEET 27 OF	SIZE C DWG. NO. LBD1829 REV

PDF-003

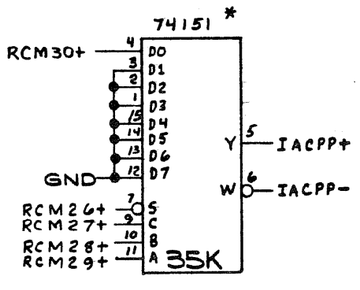
PRIME COMPUTER, INC.



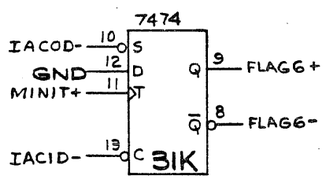
III-28

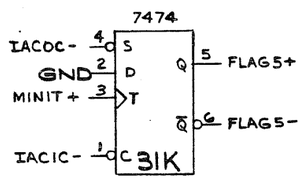
* NEED S IN HIGH SPEED MPC

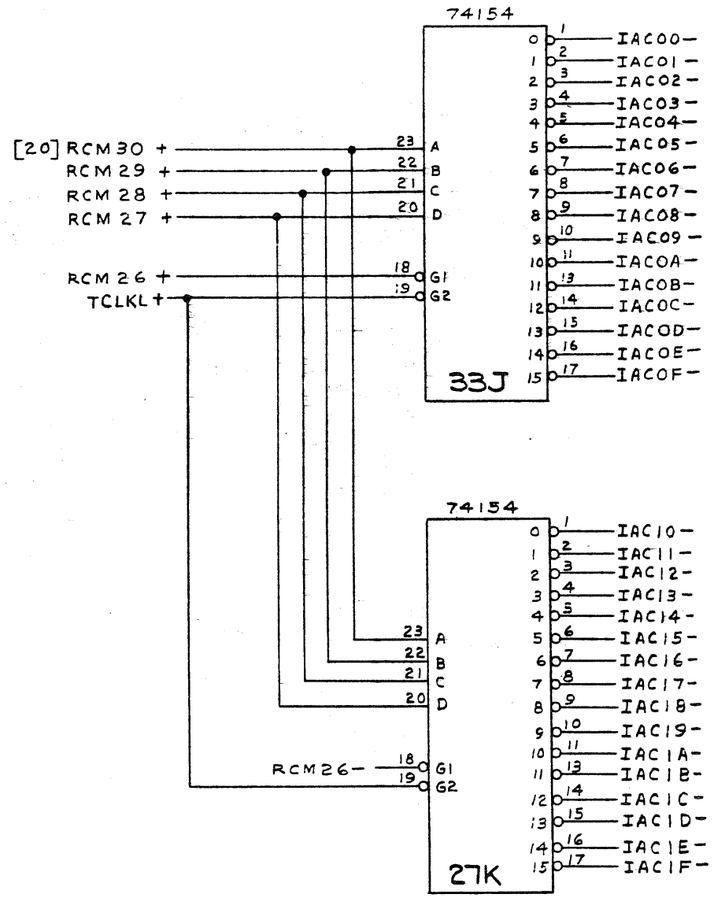
MATERIAL	DWN H. H. R 4/2/73	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	OPTION MPC-2 (EV) U-PROGRAMMED CONTROLLER JUMP NET
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 28 OF — SIZE C — DWG. NO. LBD1829M — REV. A



POP IAC



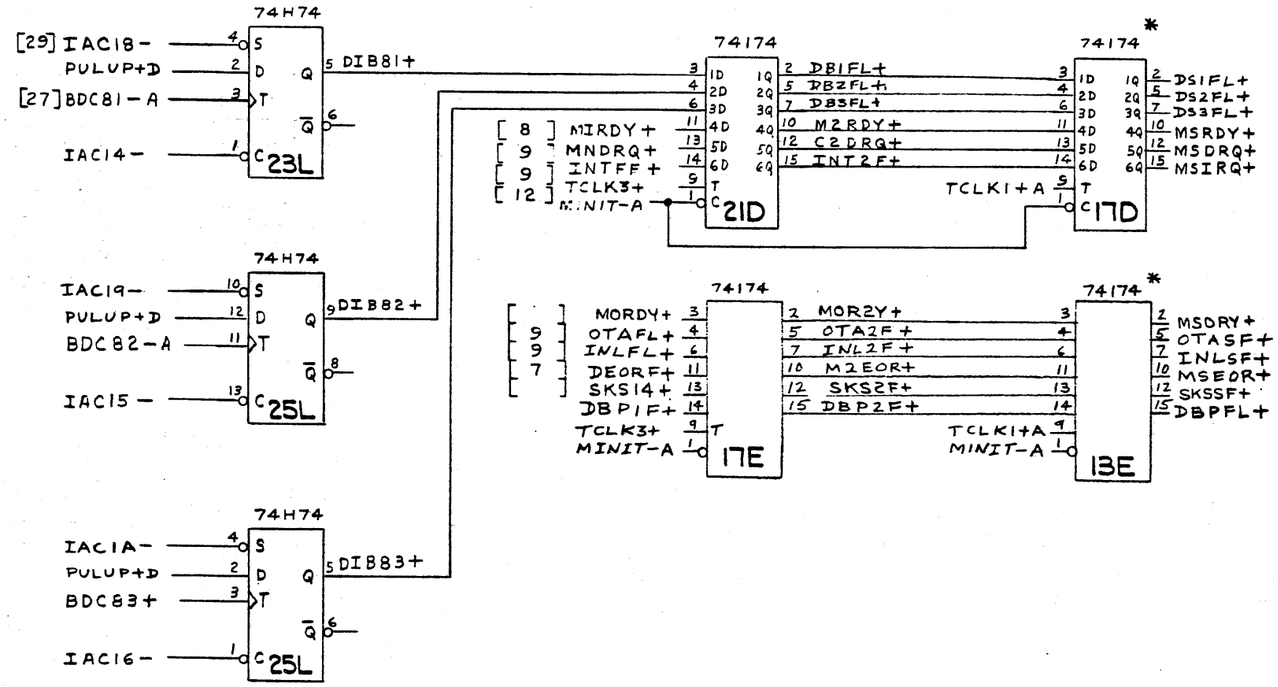




* NEED S IN HIGH SPEED MPC

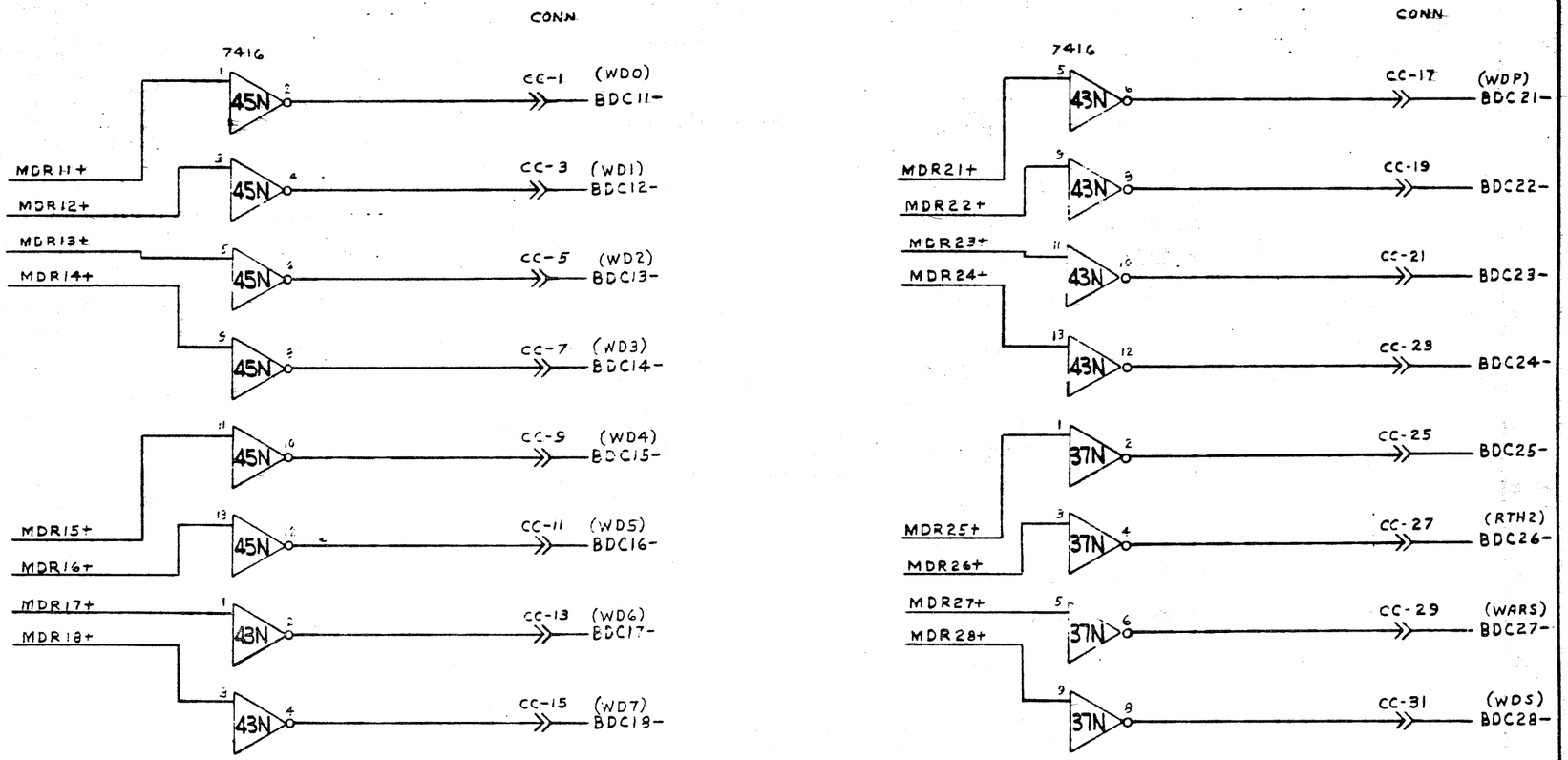
MATERIAL	DWN M.W. E 4/2/75	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ± .02 XXX ± .005 ANGLES ± 1/2°	ENG.	OPTION MPC-2 (EV) MU-PROGRAMMED CONTROLLER INDEP ACTION CODES
	APPRD	
	USED ON	SCALE: SIZE C DWG. NO. LBD1829 REV. A
	NEXT ASSY	SHEET 29 OF

Synchronizer



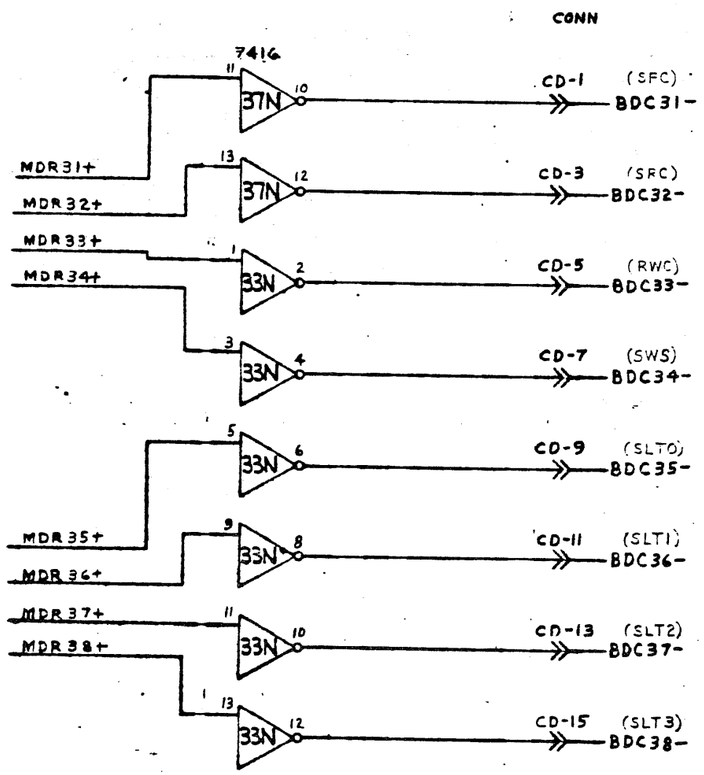
* MUST BE S IN HIGH SPEED MPC

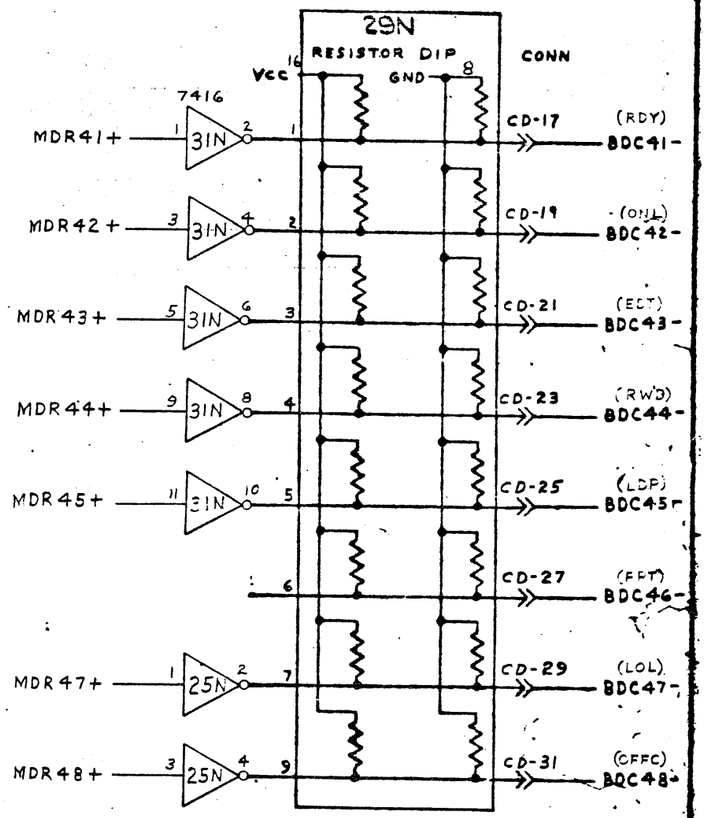
MATERIAL	DWN JH. JH. B 4/5/73	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	OPTION MPC-2 (EV) MICRO-PROGRAMMED CONTROLLER DEVICE RELATED LOGIC
	APPRD	
	USED ON / NEXT ASSY	SCALE / SHEET 30 OF
		SIZE C / DWG. NO. LBD1829 / REV. A



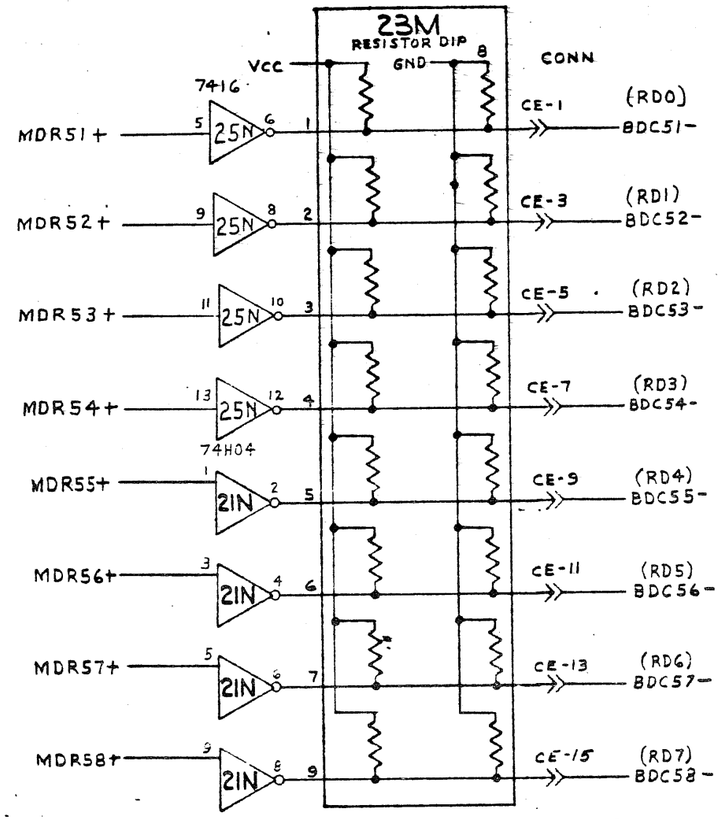
MATERIAL	DWN 7/11/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°	ENG.	MAG TAPE WRITE DATA U-PROGRAMMED CONTROLLER DEV RES OUTPUT DRIVERS
	APPRD 7-9-74	
	USED ON	SIZE C DWG. NO. LBD16291 REV. A
	NEXT ASSY	SCALE SHEET 31 OF

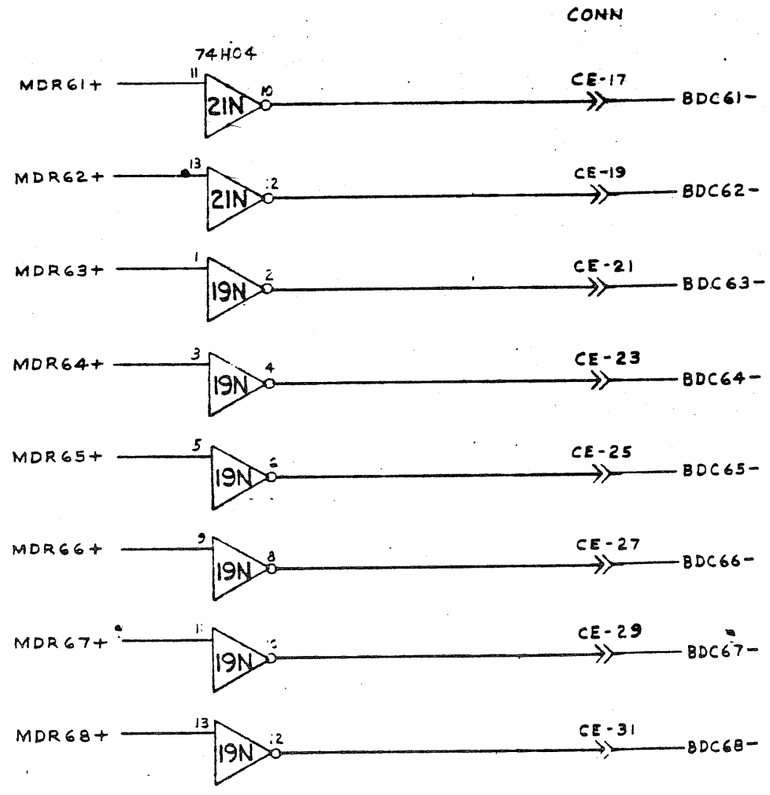
POF-003





MATERIAL	DWN H. H. B 3/23/73	PRIME COMPUTER, INC. NATICK, MASS.
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES- —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ± 1/2°	CHK	MAG TAPE CONTROL U-PROGRAMMED CONTROLLER DEV REG OUTPUT DRIVERS
	ENG.	
	APPRD 4.m 1-9-74	
	USED ON	SIZE C DWG. NO. LBD1829 REV F
	NEXT ASSY	SHEET OF





MATERIAL	DWN	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	MAG TAPE READ DATA U-PROGRAMMED CONTROLLER DEV RES OUTPUT DRIVERS
	APPRO 10-9-74	
	USED ON	SCALE — SIZE C DWG. NO. LBD1829 REV. A
	NEXT ASSY	SHEET 33A OF

PDF-003

MPC-2
DIP ALLOCATION

SHT 24 DWG NO. LBD 1829 REV A

LTR	DATE	REVISION	DR.	CK.

(SOLDER SIDE)

NAME		CONN PIN
VCC1		CA-1
VCC1		CA-2
SHIELD(GND)		CA-3
BPCDCPN+		CA-4
BPCDEN+		CA-5
GND		CA-6
BPCDPHO-		CA-7
BPCDPNA-		CA-8
BPCDPNB-		CA-9
BPCDPNC-		CA-10
BPCDPND-		CA-11
BPCDPNE-		CA-12
BPCDPNF-		CA-13
BPCDPNG-		CA-14
BPCDPNH-		CA-15
BPCIIN+		CA-16
BPCIPHO-		CA-17
BPCIPNA-		CA-18
BPCIPNB-		CA-19
BPCIPNC-		CA-20
BPCIPND-		CA-21
SHIELD(GND)		CA-22
BPCIOPN+		CA-23
GND		CA-24
BPCEHI+		CA-25
SHIELD(GND)		CA-26
		CA-27
		CA-28
		CA-29
BPCEOR+		CA-30
		CA-31
		CA-32
		CA-33
		CA-34
		CA-35
		CA-36
		CA-37
BPCIOVI-		CA-38
		CA-39
		CA-40
		CA-41
GND		CA-42
BMCWDLR+		CA-43
		CA-44
		CA-45
		CA-46
BMCWDLL+		CA-47
SHIELD(GND)		CA-48
VCC2		CA-49
VCC2		CA-50

NAME		CONN PIN
BMCABL+		CA-51
		CA-52
		CA-53
		CA-54
		CA-55
BMAPEL+		CA-56
BMAPER+		CA-57
BMDPEL-		CA-58
BMDPER-		CA-59
GND		CA-60
BMDD01+		CA-61
BMDD02+		CA-62
BMDD03+		CA-63
BMDD04+		CA-64
BMDD05+		CA-65
BMDD06+		CA-66
BMDD07+		CA-67
BMDD08+		CA-68
BMDD09+		CA-69
BMDD10+		CA-70
BMDD11+		CA-71
BMDD12+		CA-72
BMDD13+		CA-73
BMDD14+		CA-74
BMDD15+		CA-75
BMDD16+		CA-76
BMDELP-		CA-77
BMDERP-		CA-78
BMCBELB-		CA-79
BMCBELT-		CA-80
BMCMSELB-		CA-81
BMCBELV-		CA-82
BMCBDINH-		CA-83
BMCCLRB-		CA-84
BMCDNLB-		CA-85
BMCREFSH-		CA-86
BMCBELC1-		CA-87
BMCMWSRB-		CA-88
BMCBEVS2-		CA-89
BMCFCLK+		CA-90
BMCGSD1-		CA-91
BMCCRA+		CA-92
BMCGSD2-		CA-93
BMCDRA+		CA-94
BMCGSD3-		CA-95
BMCPNCH-		CA-96
BMCCNBL-		CA-97
GND		CA-98
VCC2		CA-99
VCC2		CA-100

NAME		CONN PIN
VCC1		CB-1
VCC1		CB-2
GND		CB-3
ISOLPARE		CB-4
BMA99-		CB-5
BMA00-		CB-6
BMA01-		CB-7
BMA02-		CB-8
BMA03-		CB-9
BMA04-		CB-10
BMA05-		CB-11
BMA06-		CB-12
BMA07-		CB-13
BMA08-		CB-14
BMA09-		CB-15
BMA10-		CB-16
BMA11-		CB-17
BMA12-		CB-18
BMA13-		CB-19
BMA14-		CB-20
BMA15-		CB-21
BMA16-		CB-22
BMALP-		CB-23
BMARP-		CB-24
DENREL-		CB-25
GND		CB-26
VCORE1		CB-27
VCORE1		CB-28
BPAC1+		CB-29
GND		CB-30
BPAC2+		CB-31
BPAD3+		CB-32
BPAC4+		CB-33
BPAD5+		CB-34
BPAD6+		CB-35
BPAD7+		CB-36
BPAD8+		CB-37
BPAD9+		CB-38
BPAC10+		CB-39
BPAD11+		CB-40
HSYSCLR-		CB-41
GND		CB-42
VCORE2		CB-43
VCORE2		CB-44
BPDPEL-		CB-45
GND		CB-46
BPDPER-		CB-47
BPA-EL-		CB-48
BPA99+		CB-49
BPAD0+		CB-50

NAME		CONN PIN
BPAI2+		CB-51
BPAI3+		CB-52
BPAI4+		CB-53
BPAI5+		CB-54
BPAI6+		CB-55
BPAIP+		CB-56
GND		CB-57
BPARP+		CB-58
BPCEIO+		CA-59
BPAPER-		CA-60
BPCBCO+		CA-61
BPCREDY-		CA-62
BPDLP+		CA-63
		CA-64
BPDD01+		CB-65
BPERP+		CB-66
BPDD02+		CB-67
BPDD03+		CB-68
BPDD04+		CB-69
BPDD05+		CB-70
BPDD06+		CB-71
BPDD07+		CB-72
BPDD08+		CB-73
BPDD09+		CB-74
BPDI0+		CB-75
BPDI1+		CB-76
I/2-		CB-77
I/2-		CB-78
BPDI2+		CB-79
BPDI3+		CB-80
BPDI4+		CB-81
BPDI5+		CB-82
BPDI6+		CB-83
BPDI7+		CB-84
BPMSBI+		CB-85
BPMSBO+		CB-86
BPMSBI+		CB-87
BPLSBO+		CB-88
BPLSBI+		CB-89
BP SCLK+		CA-90
I/2+		CB-91
I/2+		CB-92
HRUN-		CB-93
HRUN-		CB-94
BPCSTRB+		CB-95
GND		CB-96
VSS		CB-97
VSS		CB-98
VBB		CB-99
VBB		CB-100

(SOLDER SIDE)

NAME		CONN PIN
BDC11-		CC-1
GND		CC-2
BDC12-		CC-3
GND		CC-4
BDC13-		CC-5
GND		CC-6
BDC14-		CC-7
GND		CC-8
BDC15-		CC-9
GND		CC-10
BDC16-		CC-11
GND		CC-12
BDC17-		CC-13
GND		CC-14
BDC18-		CC-15
GND		CC-16
BDC21-		CC-17
GND		CC-18
BDC22-		CC-19
GND		CC-20
BDC23-		CC-21
GND		CC-22
BDC24-		CC-23
GND		CC-24
BDC25-		CC-25
GND		CC-26
BDC26-		CC-27
GND		CC-28
BDC27-		CC-29
GND		CC-30
BDC28-		CC-31
GND		CC-32
BDC71-		CC-33
GND		CC-34
BDC72-		CC-35
GND		CC-36
BDC73-		CC-37
GND		CC-38
BDC74-		CC-39
GND		CC-40
BDC75-		CC-41
GND		CC-42
		CC-43
		CC-44

NAME		CONN PIN
BDC31-		CD-1
GND		CD-2
BDC32-		CD-3
GND		CD-4
BDC33-		CD-5
GND		CD-6
BDC34-		CD-7
GND		CD-8
BDC35-		CD-9
GND		CD-10
BDC36-		CD-11
GND		CD-12
BDC37-		CD-13
GND		CD-14
BDC38-		CD-15
GND		CD-16
BDC41-		CD-17
GND		CD-18
BDC42-		CD-19
GND		CD-20
BDC43-		CD-21
GND		CD-22
BDC44-		CD-23
GND		CD-24
BDC45-		CD-25
GND		CD-26
BDC46-		CD-27
GND		CD-28
BDC47-		CD-29
GND		CD-30
BDC48-		CD-31
GND		CD-32
BDC76-		CD-33
GND		CD-34
BDC77-		CD-35
GND		CD-36
BDC78-		CD-37
GND		CD-38
BDC81-		CD-39
GND		CD-40
BDC82-		CD-41
GND		CD-42
		CD-43
		CD-44

NAME		CONN PIN
BDC51-		CE-1
GND		CE-2
BDC52-		CE-3
GND		CE-4
BDC53-		CE-5
GND		CE-6
BDC54-		CE-7
GND		CE-8
BDC55-		CE-9
GND		CE-10
BDC56-		CE-11
GND		CE-12
BDC57-		CE-13
GND		CE-14
BDC58-		CE-15
GND		CE-16
BDC61-		CE-17
GND		CE-18
BDC62-		CE-19
GND		CE-20
BDC63-		CE-21
GND		CE-22
BDC64-		CE-23
GND		CE-24
BDC65-		CE-25
GND		CE-26
BDC66-		CE-27
GND		CE-28
BDC67-		CE-29
GND		CE-30
BDC68-		CE-31
GND		CE-32
BDC83-		CE-33
GND		CE-34
BDC84-		CE-35
GND		CE-36
BDC85-		CE-37
GND		CE-38
BDC86-		CE-39
GND		CE-40
BDC87-		CE-41
GND		CE-42
BDC88-		CE-43
GND		CE-44

NAME		CONN PIN
5V+		CF-1
GND		CF-2
GND		CF-3
GND		CF-4
—		CF-5
—		CF-6
—		CF-7
GND		CF-8
—		CF-9
—		CF-10
—		CF-11
—		CF-12
—		CF-13
—		CF-14
—		CF-15
—		CF-16
—		CF-17
SWSTR+		CF-18
—		CF-19
—		CF-20
—		CF-21
—		CF-22
—		CF-23
—		CF-24
—		CF-25
SWSCG+		CF-26
TCLIA-		CF-27
GND		CF-28
SWSYG+		CF-29
MINIT-E		CF-30
MCY16+		CF-31
MCY05+		CF-32
MCY15+		CF-33
MCY06+		CF-34
MCY14+		CF-35
MCY07+		CF-36
MCY13+		CF-37
MCY08+		CF-38
MCY12+		CF-39
MCY09+		CF-40
MCY11+		CF-41
MCY10+		CF-42
GND		CF-43
5V+		CF-44

MATERIAL	DWN M. Bogan 8/8/74	PRIME COMPUTER, INC. NATICK, MASS.
	CHK	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	ENG.	CONNECTOR SIGNAL(E.V.) NAME LIST, MPC2
	APPRD	
	USED ON / NEXT ASSY	SCALE —— SIZE C DWG. NO. LBD1829 REV. A
		SHEET 35 OF

A B C D E F G H J K L M N P R S T V W X Y

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

CABLE J103, READ DATA, MPC CONN E

SIGNAL NAME			PRIME		TAPE TRANSPORT	
TRANSPORT	PRIME	LBD	SIG	GND	SIG	GND
RD0	BDC51-	33A	1	2	B	C
RD1	BDC52-	33A	3	4	4	D
RD2	BDC53-	33A	5	6	8	J
RD3	BDC54-	33A	7	8	9	K
RD4	BDC55-	33A	9	10	14	R
RD5	BDC56-	33A	11	12	15	S
RD6	BDC57-	33A	13	14	17	U
RD7	BDC58-	33A	15	16	18	V
			17	18		
			19	20		
			21	22		
			23	24		
			25	26		
			27	28		
			29	30		
			31	32		
RDS	BDC83-	27A	33	34	2	B
			35	36		
			37	38		
			39	40		
RDP	BDC87-	27A	41	42	1	A
			43	44		

CABLE J102, WRITE DATA, MPC CONN C

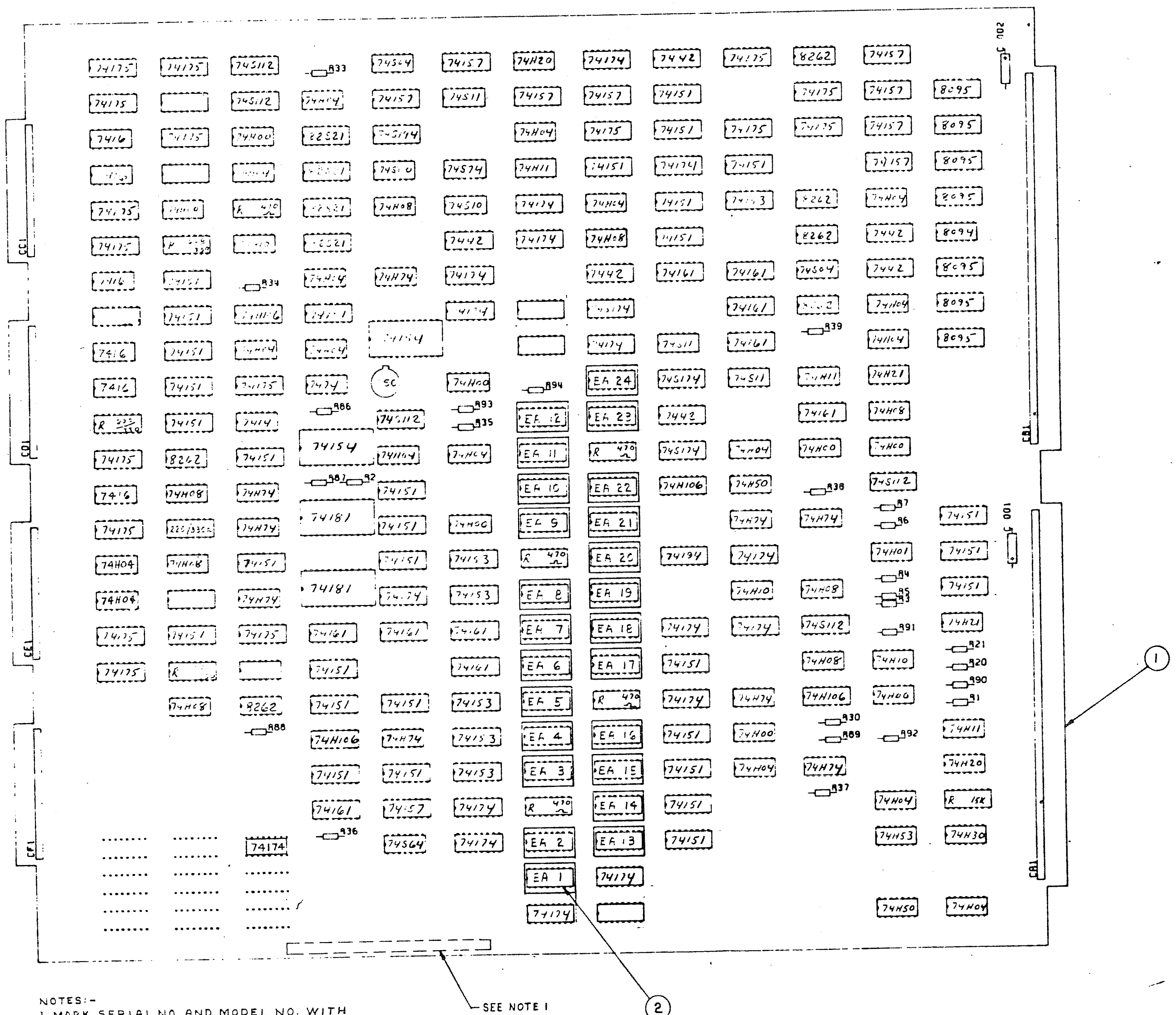
SIGNAL NAME			PRIME		TAPE TRANSPORT	
TRANSPORT	PRIME	LBD	SIG	GND	SIG	GND
WD0	BDC11-	31A	1	2	M	11
WD1	BDC12-	31A	3	4	N	12
WD2	BDC13-	31A	5	6	P	13
WD3	BDC14-	31A	7	8	R	14
WD4	BDC15-	31A	9	10	S	15
WD5	BDC16-	31A	11	12	T	16
WD6	BDC17-	31A	13	14	U	17
WD7	BDC18-	31A	15	16	V	18
WDP	BDC21-	31A	17	18	L	10
			19	20		
			21	22		
			23	24		
			25	26		
RTH2	BDC26-	31A	27	28	F	6
WARS	BDC27-	31A	29	30	C	3
WDS	BDC28-	31A	31	32	A	1
			33	34		
			35	36		
			37	38		
			39	40		
			41	42		
			43	44		

CABLE J101, CONTROL, MPC CONN D

SIGNAL NAME			PRIME		TAPE TRANSPORT	
TRANSPORT	PRIME	LBD	SIG	GND	SIG	GND
SFC	BDC31-	32A	1	2	C	3
SRC	BDC32-	32A	3	4	E	5
RWC	BDC33-	32A	5	6	H	7
SWS	BDC34-	32A	7	8	K	9
SLT0	BDC35-	32A	9	10	J	8
SLT1	BDC36-	32A	11	12	A	8
SLT2	BDC37-	32A	13	14	18	8
SLT3	BDC38-	32A	15	16	V	8
RDY	BDC41-	32A	17	18	T	16
ONL	BDC42-	32A	19	20	M	11
EOT	BDC43-	32A	21	22	U	17
RWD	BDC44-	32A	23	24	N	12
LDP	BDC45-	32A	25	26	R	14
FPT	BDC46-	32A	27	28	P	13
LOL	BDC47-	32A	29	30	1	3
OFFC	BDC48-	32A	31	32	L	10
			33	34		
			35	36		
DDI	BDC78-	27A	37	38	F	6
			39	40		
			41	42		
			43	44		

MATERIAL	DWN Sr. Tech Dan 3/4/74	PRIME COMPUTER, INC. NATICK, MASS.	
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ±.02 .XXX ±.005 ANGLES ±1/2°	CHK 10/9/74	MAG TAPE MNUEMONIC CROSS REF CHART	M
	ENG.		
	APPRD 10-9-74		
	USED ON / NEXT ASSY	SCALE / SHEET 36 OF	SIZE C / DWG. NO. LBD1829 / REV. A

LTR	DATE	REVISION	DR.	CK.
A		RELEASED		
B		ADDED ETCH CUT PER ECN 1533	PB	



NOTES:-
1. MARK SERIAL NO. AND MODEL NO. WITH APPROPRIATE REV IN WHITE INK. LOCATE APPROX AS SHOWN.

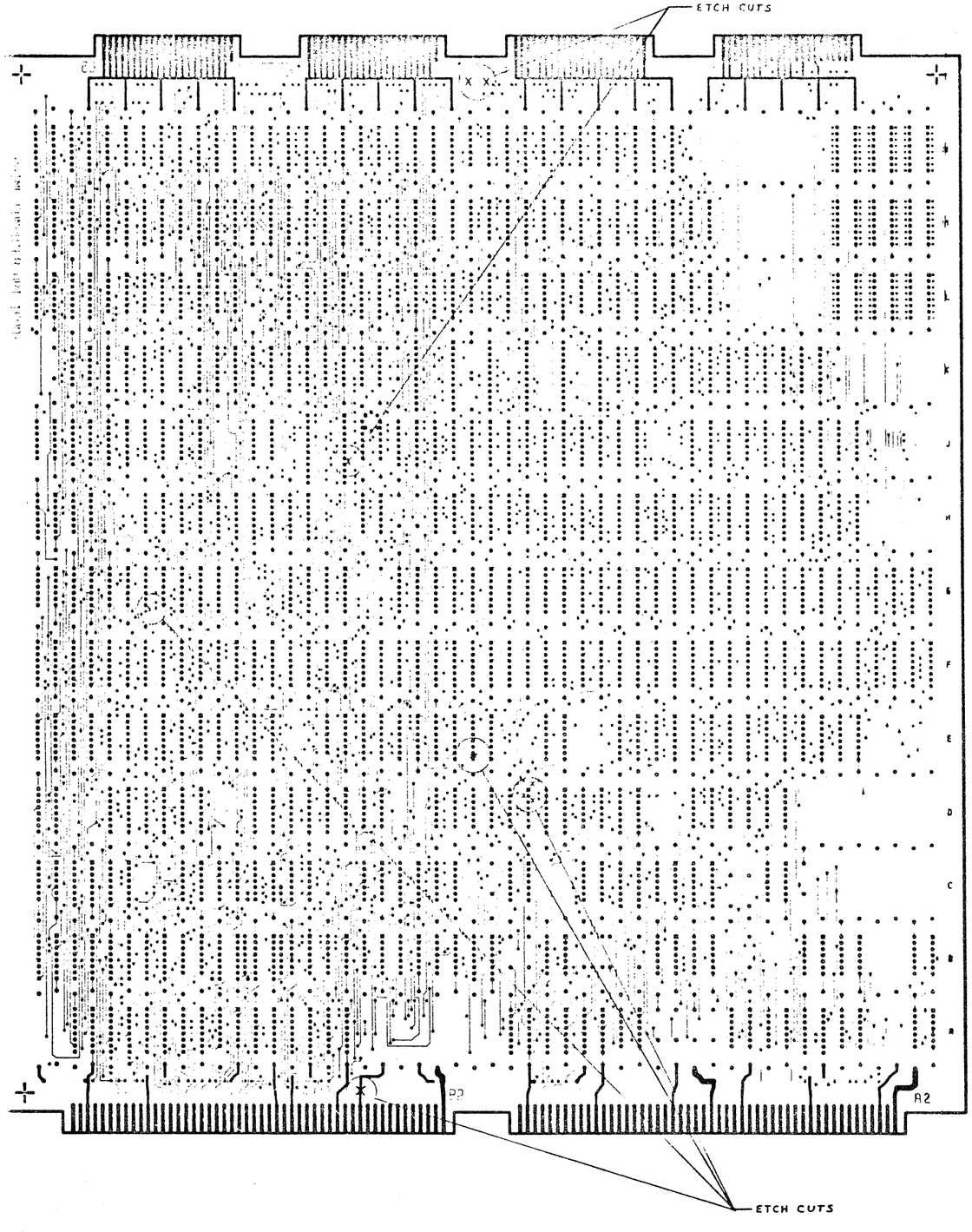
PRIME COMPUTER INC.
NATICK, MASS.

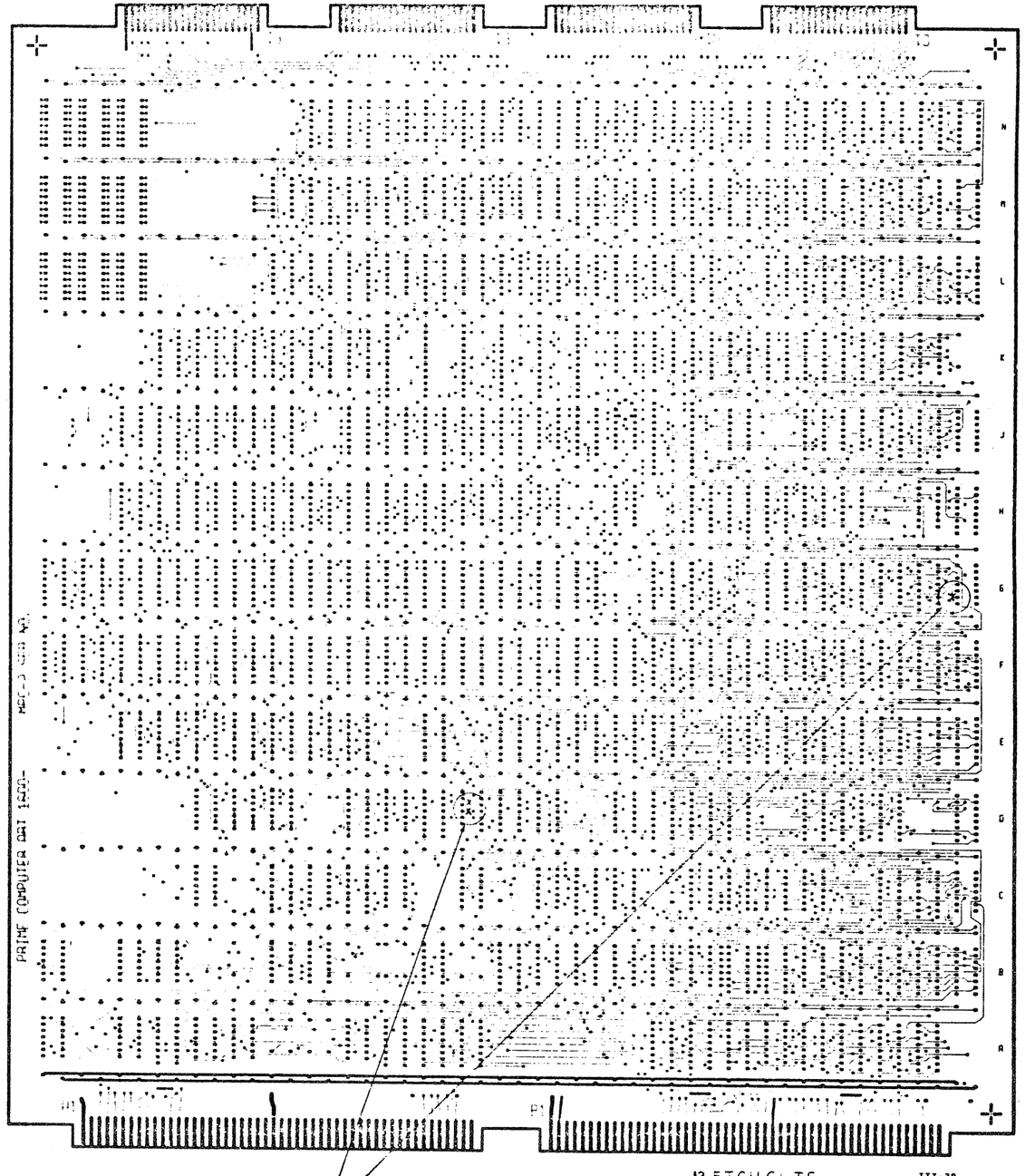
CONTROLLER ASSY
MAG TAPE

EV

SIZE	DWG. NO.	REV.
D	4020-002	B

SCALE 1/1 SHEET 1 OF 1





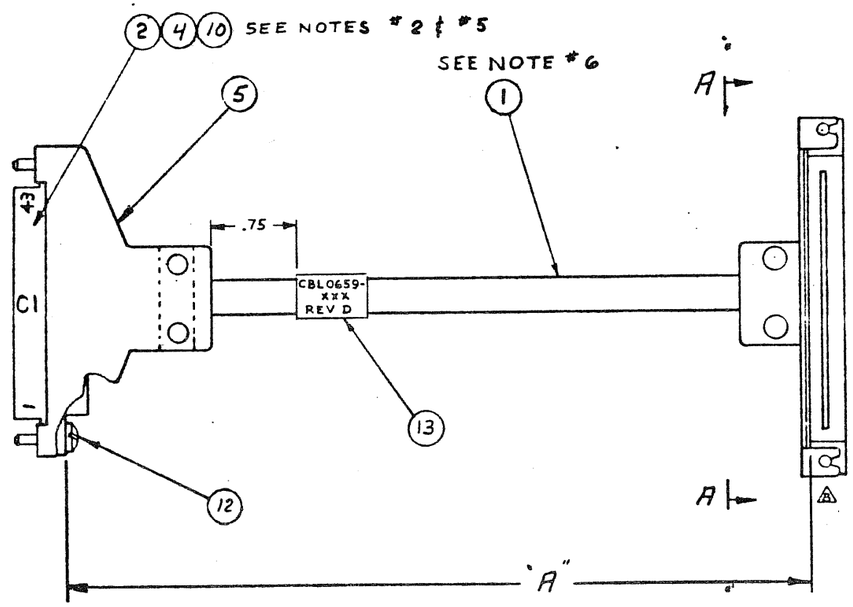
12 ETCH CUTS

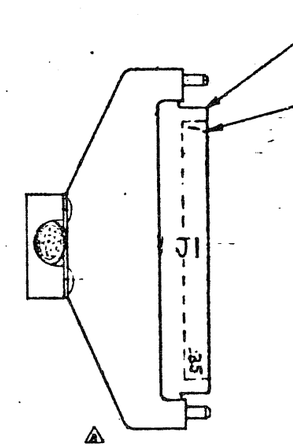
III-38

MATERIAL: MAKE FROM PCB 1601	DWN: 9/11/74	PRIME COMPUTER INC. NATICK, MASS.	
	ENG: 10/3/74	PC BOARD ETCH CUTS MPC 2 EV	
	APPRD: 10-9-74		
	USED ON: NEXT ASSY MEC2040	SCALE: NONE SHEET 1 OF 1	SIZE D DWG NO MEC1849-001 REV B

REVISION			
-	7/13	RELEASED	JCL
A		REVISED PER ECN 1206	JCL
C	9/1/73	REVISED PER ECN 1210	WB JCL
D	1/8/74	PER ECN 1520 & 1312	WB JCL

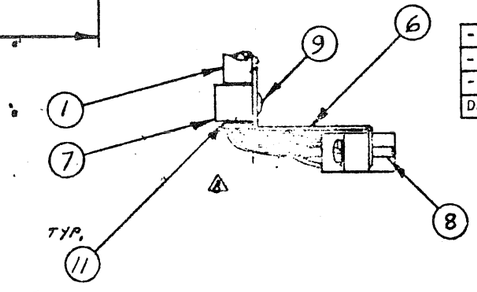
WIRE LIST			COMMENTS
FROM	TO	COLOR	
C1-1	J1-6	BLK	TWISTED PAIR
C1-2	J1-5	WHT	
C1-3	J1-10	YEL	
C1-4	J1-9	ORN	
C1-5	J1-14	GRN	
C1-6	J1-13	GRY	
C1-7	J1-18	BLK/WHT	
C1-8	J1-17	BLK/RED	
C1-9	J1-16	BLK/GRN	
C1-10	J1-15*	BLK/ORN	
C1-11	J1-2	BLK/YEL	
C1-12	J1-15*	BLK/BLU	
C1-13	J1-35	WHT/BLK	
C1-14	J1-15*	WHT/RED	
C1-15	J1-36	WHT/GRN	
C1-16	J1-15*	WHT/ORN	
C1-17	J1-32	WHT/BLU	
C1-18	J1-31	WHT/YEL	
C1-19	J1-22	WHT/BRN	
C1-20	J1-21	WHT/GRY	
C1-21	J1-34	YEL/BLK	
C1-22	J1-33	YEL/RED	
C1-23	J1-24	YEL/GRN	
C1-24	J1-23	YEL/BLU	
C1-25	J1-28	YEL/BRN	
C1-26	J1-27	YEL/GRY	
C1-27	J1-26	ORN/BLK	
C1-28	J1-25	ORN/RED	
C1-29	J1-1	ORN/GRN	
C1-30	J1-3	ORN/BLU	
C1-31	J1-20	ORN/GRN	
C1-32	J1-19	ORN/GRY	
C1-37	J1-12	GRN/BRN	TWISTED PAIR
C1-38	J1-11	GRN/YEL	





VIEW A-A

1/2 & 3/4	WANG
5/4 & 7/8	PERTEC
KEY SLOT REF TABLE	MTT



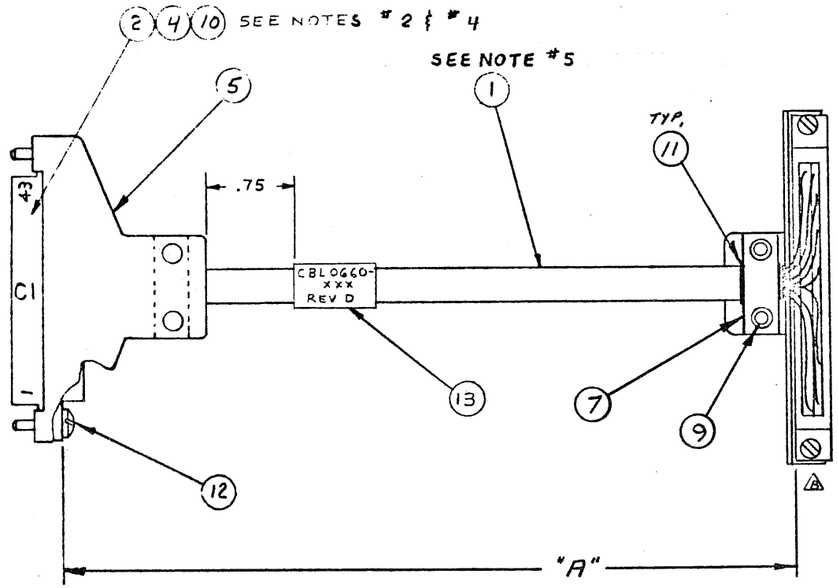
-003	30 FT	± 1 FT
-002	12 FT	± 6"
-001	4 FT	± 6"
DASH NO.	DIM A	TOL.

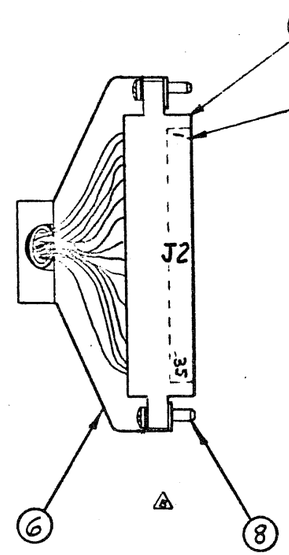
NOTES:
1. STAMP MARKINGS C1 AND J1 .19 HIGH IN WHITE INK. LOCATE APPROX AS SHOWN.
2. INSERT KEY, ITEM #10 BETWEEN SLOTS 25/26 & 27/28 OF ITEM #2
3. INSERT KEY, ITEM #10 AT J1 CONN DURING SYSTEM CONFIGURATION. LOCATE KEY PER REF TABLE.
4. * PIGTAIL FOUR WIRES INDICATED TO J1-15
5. SEE DRAWING INS1210 FOR CABLE CODING LOCATION.
6. ALL UNUSED WIRES ARE TO BE TERMINATED INSIDE CABLE. (CUT-OFF AT BOTH ENDS)

MATERIAL: SEE BOM	DRAWN 7/24/73 CHK 11/13/75	SIZE D
		CABLE, MAGNETIC TAPE CONTROLLER (CONTROL)

WIRE LIST			COMMENT
FROM	TO	COLOR	
C1-1	J2-22	BLK	TWISTED PAIR
C1-2	J2-21	WHT	
C1-3	J2-24	YEL	
C1-4	J2-23	ORN	
C1-5	J2-26	GRN	
C1-6	J2-25	GRY	
C1-7	J2-28	BLK/WHT	
C1-8	J2-27	BLK/RED	
C1-9	J2-30	BLK/GRN	
C1-10	J2-29	BLK/ORN	
C1-11	J2-32	BLK/YEL	
C1-12	J2-31	BLK/BLU	
C1-13	J2-34	WHT/BLK	
C1-14	J2-33	WHT/RED	
C1-15	J2-36	WHT/GRN	
C1-16	J2-35	WHT/ORN	
C1-17	J2-20	WHT/BLU	
C1-18	J2-19	WHT/YEL	
C1-27	J2-12	GRN/BLK	
C1-28	J2-11	ORN/RED	
C1-29	J2-6	ORN/GRN	
C1-30	J2-5	ORN/BLU	
C1-31	J2-2	ORN/BRN	
C1-32	J2-1	GRN/GRY	TWISTED PAIR
			TWISTED PAIR

LTR	DATE	REVISION	BY	CK
A	7/24/73	RELEASED	J.C.T.	J.G.H.
B	9/28/73	REVISED PER ECN 1206	J.C.T.	J.G.H.
C	12/1/73	REVISED PER ECN 1210	K.B.	J.G.H.
D	1/8/75	PER ECO 1520 & 1312	K.B.	J.G.H.





-003	30 FT.	± 1 FT.
-002	12 FT.	± 6"
-001	4 FT.	± 6"
-XXX	"A"	TOL

NOTES:
1. STAMP MARKINGS C1 AND J2 .19 HIGH IN WHITE INK. LOCATE APPROX AS SHOWN.
2. INSERT KEY, ITEM #10 BETWEEN SLOTS 25/26 & 27/28 OF ITEM #2
3. INSERT KEY, ITEM #10 BETWEEN SLOTS 9/10 & 11/12 OF ITEM #3
4. SEE DRAWING INS1210 FOR CABLE CODING INSTRUCTIONS.
5. ALL UNUSED WIRES ARE TO BE TERMINATED INSIDE CABLE. (CUT-OFF AT EACH END)

MATERIAL: SEE BOM

UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES .XX ± .02 .XXX ± .005 ANGLES ± 1/2°

DWN J.C.T. 7/24/73
CHK J.G.H. 1/10/75
ENG.
APPRD
USED ON
NEXT ASSY 4141/4143

PRIME COMPUTER, INC.
NATICK, MASS.

CABLE, MAGNETIC TAPE CONTROLLER (WRITE DATA) CONN. C

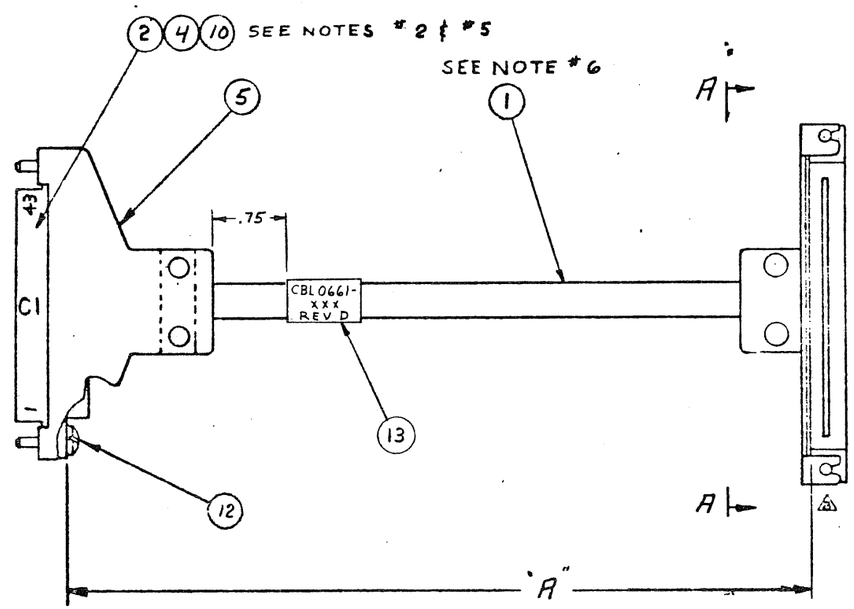
SCALE NONE | SIZE C | DWG NO CBL0660-XXX | REV D

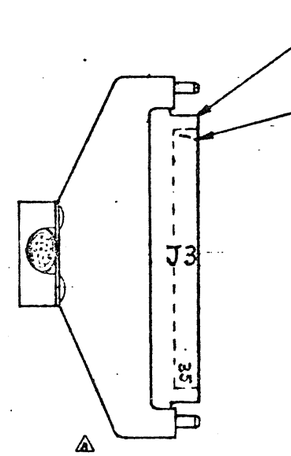
SHEET 1 OF 1

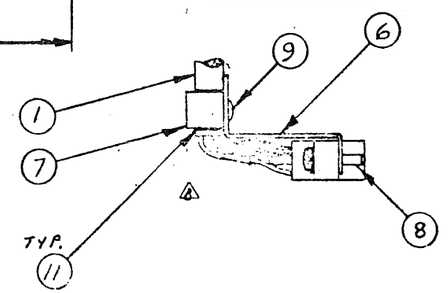
CBL0660-XXX D

WIRE LIST			COMMENTS
FROM	TO	COLOR	
C1-1	J3-5	BLK	TWISTED PAIR
C1-2	J3-6	WHT	
C1-3	J3-7	YEL	
C1-4	J3-8	ORN	
C1-5	J3-15	GRN	
C1-6	J3-16	GRY	
C1-7	J3-17	BLK/WHT	
C1-8	J3-18	BLK/RED	
C1-9	J3-27	BLK/GRN	
C1-10	J3-28	BLK/ORN	
C1-11	J3-29	BLK/YEL	
C1-12	J3-30	BLK/BLU	
C1-13	J3-33	WHT/BLK	
C1-14	J3-34	WHT/RED	
C1-15	J3-35	WHT/GRN	
C1-16	J3-36	WHT/ORN	
C1-33	J3-3	GRN/BLK	
C1-34	J3-4	GRN/RED	
C1-41	J3-1	GRY/RED	TWISTED PAIR
C1-42	J3-2	GRY/WHT	

LTR	DATE	REVISION	DR.	CK.
A	2/24/73	RELEASED	JCH	JCH
B	7/6/73	REVISED PER ECN 1206	JCH	JCH
C	10/1/73	REVISED PER ECN 1210	WB	JCH
D	11/8/75	PER ECO 1520 & 1312	WB	JCH







-003	30FT	± 1FT
-002	12 FT	± 6"
-001	4 FT	± 6"
-XXX	"A"	TOL.

NOTES:
1. STAMP MARKINGS C1 AND J3 .19 HIGH IN WHITE INK. LOCATE APPROX AS SHOWN.
2. INSERT KEY, ITEM #10 BETWEEN SLOTS 25/26 & 27/28 OF ITEM #2
3. INSERT KEY, ITEM #10 BETWEEN SLOTS 5/6 & 7/8 OF ITEM #3
4
5. SEE DRAWING INS1210 FOR CABLE ROUTING LOCATION.
6. ALL UNUSED WIRES ARE TO BE TERMINATED INSIDE CABLE. (CUT-OFF AT BOTH ENDS)

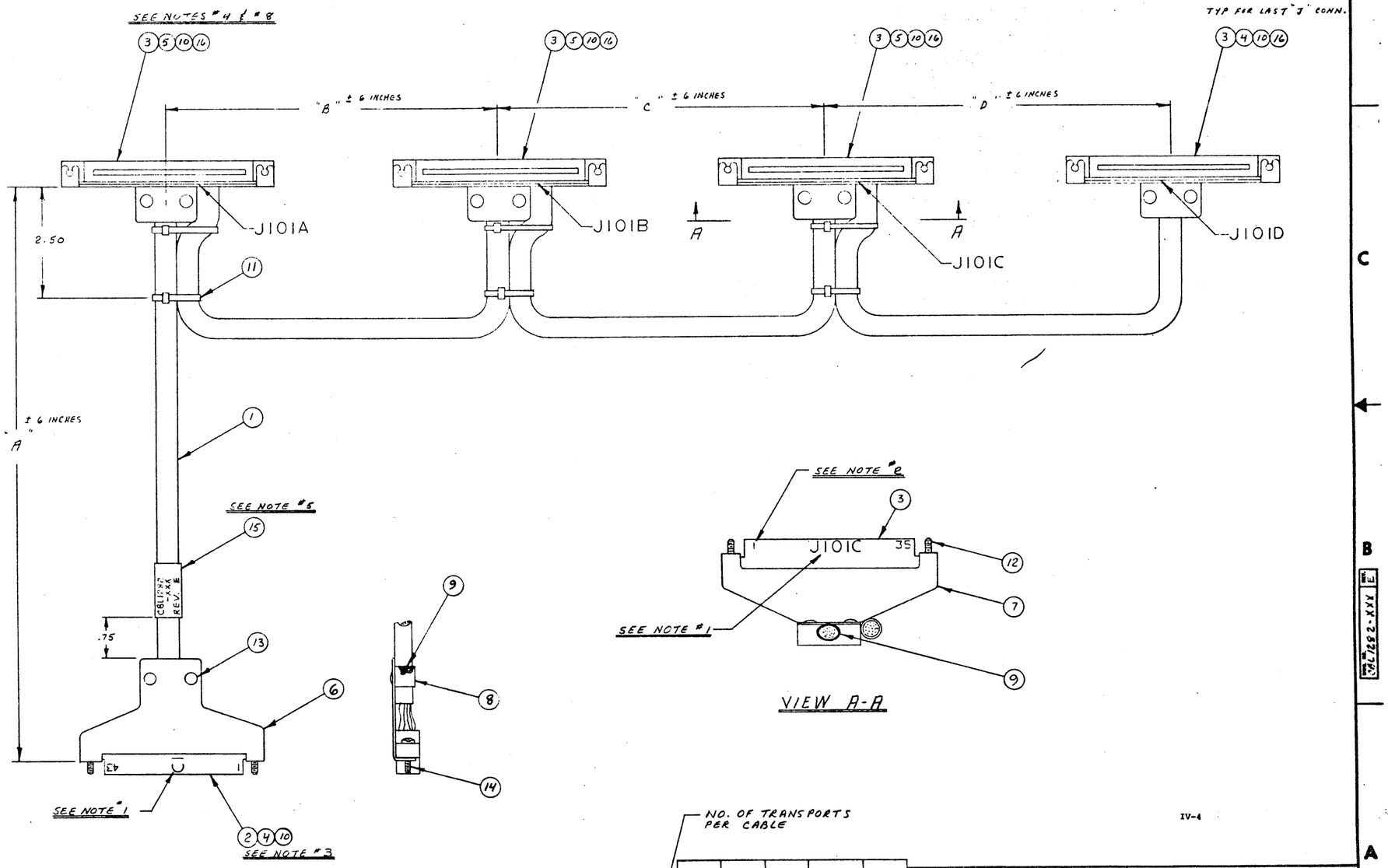
MATERIAL: SEE BOM	DRAWN 2/24/73 JCH	PRIME COMPUTER, INC.
	CHECKED 11/10/75	CABLE, MAGNETIC TAPE CONTROLLER (READ DATA) CONN, F
		0661-XXX D

LTR	DATE	REVISION	DR.	CK.
D	[illegible]	[illegible] 1432	[illegible]	[illegible]
E	[illegible]	[illegible] 1520 (NOTE 4)	[illegible]	[illegible]

WIRE LIST

FROM	TO	TO	TO	TO	COLOR	COMMENTS
C1-1	J101A-6	J101B-6	J101C-6	J101D-6	BLK	TWISTED PAIR
C1-2	J101A-5	J101B-5	J101C-5	J101D-5	WHT	
C1-3	J101A-10	J101B-10	J101C-10	J101D-10	YEL	
C1-4	J101A-9	J101B-9	J101C-9	J101D-9	ORN	
C1-5	J101A-14	J101A-14	J101C-14	J101D-14	GRN	
C1-6	J101A-13	J101A-13	J101C-13	J101D-13	GRY	
C1-7	J101A-18	J101A-18	J101C-18	J101D-18	BLK	WHT
C1-8	J101A-17	J101A-17	J101C-17	J101D-17	BLK	RED
C1-9	J101A-16	J101B-16	J101C-16	J101D-16	BLK	GRN
C1-10	J101A-*15	J101B-*15	J101C-*15	J101D-*15	BLK	ORN
C1-11	J101A-2	J101B-2	J101C-2	J101D-2	BLK	YEL
C1-12	J101A-*15	J101B-*15	J101C-*15	J101D-*15	BLK	BLU
C1-13	J101A-35	J101B-35	J101C-35	J101D-35	WHT	BLK
C1-14	J101A-*15	J101B-*15	J101C-*15	J101D-*15	WHT	RED
C1-15	J101A-36	J101B-36	J101C-36	J101D-36	WHT	GRN
C1-16	J101A-*15	J101B-*15	J101C-*15	J101D-*15	WHT	ORN
C1-17	J101A-32	J101B-32	J101C-32	J101D-32	WHT	BLU
C1-18	J101A-31	J101B-31	J101C-31	J101D-31	WHT	YEL
C1-19	J101A-22	J101B-22	J101C-22	J101D-22	WHT	BRN
C1-20	J101A-21	J101B-21	J101C-21	J101D-21	WHT	GRY
C1-21	J101A-34	J101B-34	J101C-34	J101D-34	YEL	BLK
C1-22	J101A-33	J101B-33	J101C-33	J101D-33	YEL	RED
C1-23	J101A-24	J101B-24	J101C-24	J101D-24	YEL	GRN
C1-24	J101A-23	J101B-23	J101C-23	J101D-23	YEL	BLU
C1-25	J101A-28	J101B-28	J101C-28	J101D-28	YEL	BRN
C1-26	J101A-27	J101B-27	J101C-27	J101D-27	YEL	GRY
C1-27	J101A-26	J101B-26	J101C-26	J101D-26	ORN	BLK
C1-28	J101A-25	J101B-25	J101C-25	J101D-25	ORN	RED
C1-29	J101A-1	J101B-1	J101C-1	J101D-1	ORN	GRN
C1-30	J101A-3	J101B-3	J101C-3	J101D-3	ORN	BLU
C1-31	J101A-20	J101B-20	J101C-20	J101D-20	ORN	BRN
C1-32	J101A-17	J101B-17	J101C-17	J101D-17	ORN	GRY
C1-37	J101A-12	J101B-12	J101C-12	J101D-12	GRN	BRN — TWISTED PAIR
C1-38	J101A-11	J101B-11	J101C-11	J101D-11	GRN	YEL

CBL1282-001
CBL1282-002
CBL1282-003



VIEW A-A

NOTES:

1. STAMP MARKINGS C1, J101A, J101B, J101C & J101D .19 HIGH IN WHITE INK. LOCATE APPROX. AS SHOWN.
2. STAMP NUMBERS 1 & 35 OVER END CONTACTS ON ITEMS # 3 AS SHOWN IN VIEW A-A. STAMP NUMBERS # 2 & # 36 OVER END CONTACTS ON OPPOSITE SIDE OF ITEMS # 3. MARKINGS TO BE .12 HIGH IN WHITE INK.
3. INSERT KEY (ITEM # 10) BETWEEN SLOTS 25/32 & 27/32 OF ITEM # 2.
4. INSERT KEY BETWEEN SLOTS 5/16 & 7/8 OF ITEMS # 3
5. TYPE PART NUMBER & REVISION ON ITEM # 15 AS SHOWN.
6. ALL UNUSED WIRES ARE TO BE TERMINATED INSIDE CABLE. (CUT-OFF AT BOTH ENDS)
7. SEE DWN INS1210 FOR CABLE CODING INSTRUCTIONS.
8. * USE ITEM # 16 TO PIGTAIL LEADS INDICATED BY AN ASTERISK (*) TO PIN 15 IN EACH J CONNECTOR.

NO. OF TRANSPORTS PER CABLE

4	-003	7 FT	7 FT	7 FT	7 FT
3	-002	10 FT	7 FT	7 FT	—
2	-001	10 FT	10 FT	—	—
	-XXX	"A"	"B"	"C"	"D"

IV-4

MATERIAL	SEE BOM
UNLESS OTHERWISE SPECIFIED —REMOVE ALL BURRS AND SHARP EDGES: —DIMENSIONS ARE IN INCHES —TOLERANCES XX ± .02, XXX ± .005, ANGLES ± 1/2°	
DWN	[illegible]
CHK	[illegible]
ENG.	[illegible] 10-1-74
APPRD	[illegible]
USED ON	
NEXT ASSY	[illegible]
SCALE	NONE
SHEET	OF 1

PRIME COMPUTER, INC.
NATICK, MASS.

CABLE, DAISY CHAIN- MPC-2 TO PERTEC 7 & 9 TRACK MTT CONTROL CONN. D

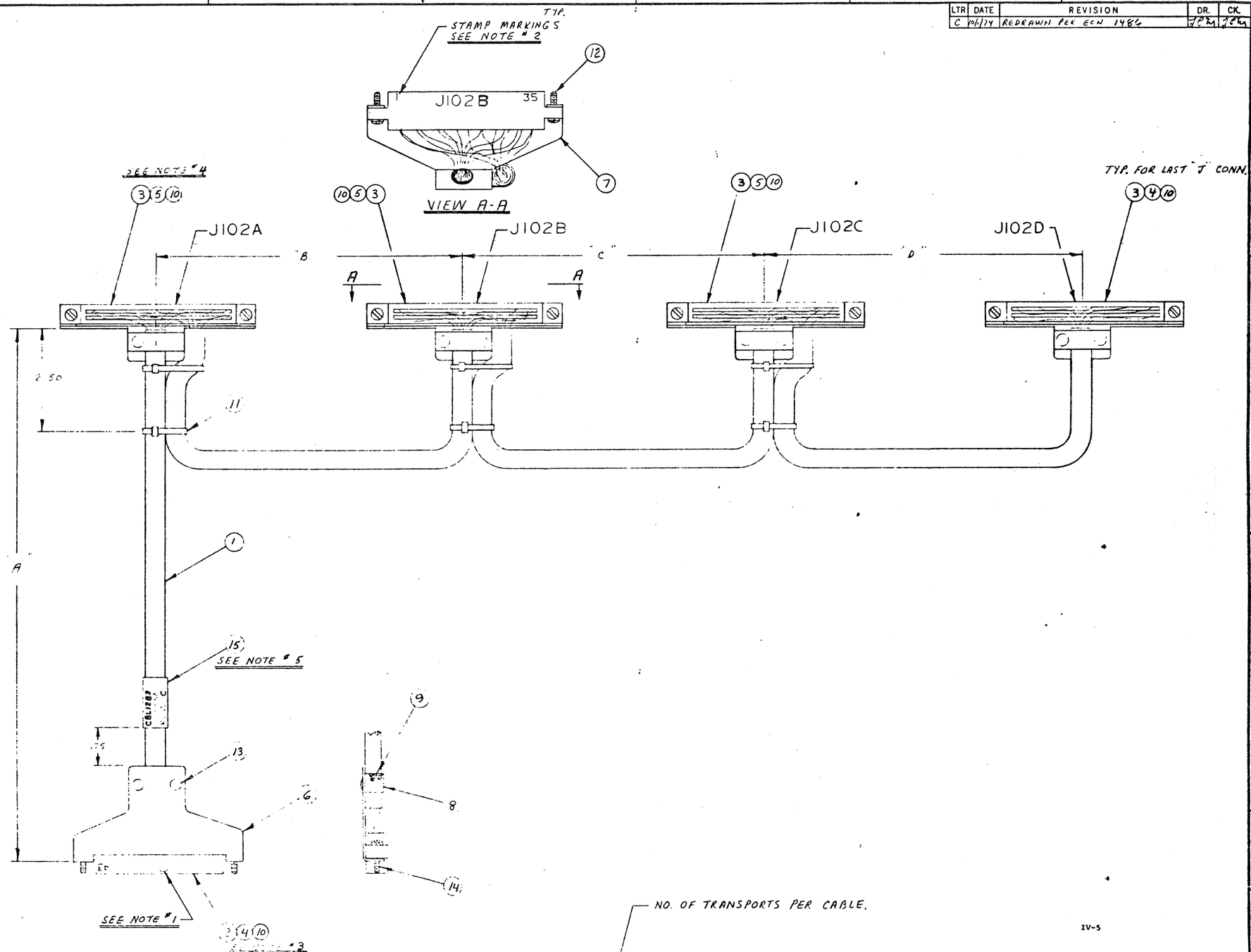
SIZE D | DWG. NO. CBL1282-XXX | REV. E

LTR	DATE	REVISION	DR.	CK.
C	10/1/74	REDRAWN PER ECN 1486	JPZ	JPZ

WIRE LIST

FROM	TO	TO	TO	TO	COLOR	COMMENTS
C1-1	J102A-22	J102B-22	J102C-22	J102D-22	BLK	TWISTED PAIR
C1-2	J102A-21	J102A-21	J102C-21	J102D-21	WHT	
C1-3	J102A-24	J102B-24	J102C-24	J102D-24	YEL	
C1-4	J102A-23	J102B-23	J102C-23	J102D-23	ORG	
C1-5	J102A-26	J102B-26	J102C-26	J102D-26	GRN	
C1-6	J102A-25	J102B-25	J102C-25	J102D-25	GRY	
C1-7	J102A-28	J102B-28	J102C-28	J102D-28	BLK	WHT
C1-8	J102A-27	J102B-27	J102C-27	J102D-27	BLK	RED
C1-9	J102A-30	J102B-30	J102C-30	J102D-30	BLK	GRN
C1-10	J102A-29	J102B-29	J102C-29	J102D-29	BLK	ORN
C1-11	J102A-32	J102B-32	J102C-32	J102D-32	BLK	YEL
C1-12	J102A-31	J102B-31	J102C-31	J102D-31	BLK	BLU
C1-13	J102A-34	J102B-34	J102C-34	J102D-34	WHT	BLK
C1-14	J102A-33	J102B-33	J102C-33	J102D-33	WHT	RED
C1-15	J102A-36	J102B-36	J102C-36	J102D-36	WHT	GRN
C1-16	J102A-35	J102B-35	J102C-35	J102D-35	WHT	ORN
C1-17	J102A-20	J102B-20	J102C-20	J102D-20	WHT	BLU
C1-18	J102A-19	J102B-19	J102C-19	J102D-19	WHT	YEL
C1-27	J102A-12	J102B-12	J102C-12	J102D-12	GRY	BLK
C1-28	J102A-11	J102B-11	J102C-11	J102D-11	GRN	RED
C1-29	J102A-6	J102B-6	J102C-6	J102D-6	ORN	GRN
C1-30	J102A-5	J102B-5	J102C-5	J102D-5	ORN	ALL
C1-31	J102A-2	J102B-2	J102C-2	J102D-2	ORN	GRN TWISTED PAIR
C1-32	J102A-1	J102B-1	J102C-1	J102D-1	GRN	GRY

CBL1233-001
CBL1233-002
CBL1233-003



NO. OF TRANSPORTS PER CABLE.

IV-5

NOTES:

1. STAMP MARKINGS C1, J102A, J102B, J102C & J102D IN WHITE INK .13 HIGH & LOCATED AS SHOWN.
2. STAMP NUMBERS 1 & 35 OVER END CONTACTS ON ITEMS #3 AS SHOWN IN VIEW A-A. STAMP NUMBERS #2 & #36 OVER END CONTACTS ON CTR. SIDE OF ITEMS #3. MARKINGS TO BE .13 HIGH IN WHITE INK.
3. INSERT KEY (ITEM #10) BETWEEN SLOTS 9/10 & 11/12 OF ITEMS #3.
4. INSERT KEY (ITEM #10) BETWEEN SLOTS 9/10 & 11/12 OF ITEMS #3.
5. TYPE PART NUMBER & REVISION ON ITEM #15 AS SHOWN.
6. ALL UNUSED WIRES ARE TO BE TERMINATED INSIDE CABLE. (CUT-OFF AT BOTH ENDS)
7. SEE DWN INS1210 FOR CABLE CODING INSTRUCTIONS.

4	7	7	7	7
3				
2				

MATERIAL

PRIME COMPUTER, INC.
NATICK, MASS.

CABLE, DAISY CHAIN, MPC-2 TO FEATEC 7 & 9 TRACK MTT WRITE DATA - CONN. C

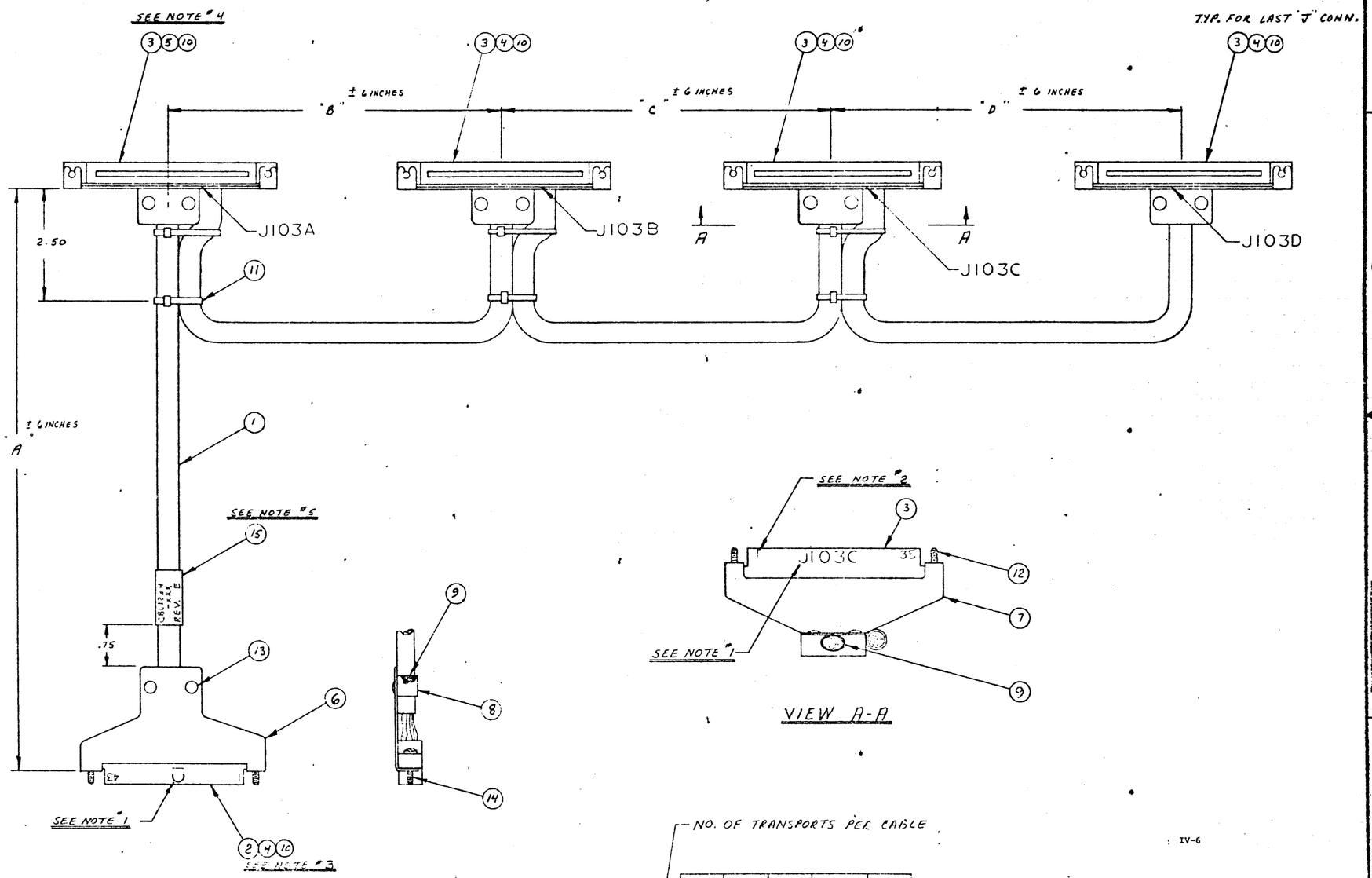
D CE-1233-XX/C

LTR	DATE	REVISION	DR.	CK.
D	7/1/74	REDRAWN PER ECN 1486	[illegible]	[illegible]
E	11/6/75	PER ECN 1520 (NOTE 4)	[illegible]	[illegible]

WIRE LIST

FROM	TO	TO	TO	TO	COLOR	COMMENTS
C1-1	J103A-5	J103B-5	J103C-5	J103D-5	BLK	TWISTED PAIR
C1-2	J103A-6	J103B-6	J103C-6	J103D-6	WHT	
C1-3	J103A-7	J103B-7	J103C-7	J103D-7	YEL	
C1-4	J103A-8	J103B-8	J103C-8	J103D-8	ORN	
C1-5	J103A-15	J103B-15	J103C-15	J103D-15	GRN	
C1-6	J103A-16	J103B-16	J103C-16	J103D-16	GRY	
C1-7	J103A-17	J103B-17	J103C-17	J103D-17	BLK / WHT	
C1-8	J103A-18	J103B-18	J103C-18	J103D-18	BLK / RED	
C1-9	J103A-27	J103B-27	J103C-27	J103D-27	BLK / GRN	
C1-10	J103A-28	J103B-28	J103C-28	J103D-28	BLK / ORN	
C1-11	J103A-29	J103B-29	J103C-29	J103D-29	BLK / YEL	
C1-12	J103A-30	J103B-30	J103C-30	J103D-30	BLK / GRY	
C1-13	J103A-33	J103B-33	J103C-33	J103D-33	WHT / BLK	
C1-14	J103A-34	J103B-34	J103C-34	J103D-34	WHT / RED	
C1-15	J103A-35	J103B-35	J103C-35	J103D-35	WHT / GRN	
C1-16	J103A-36	J103B-36	J103C-36	J103D-36	WHT / ORN	
C1-33	J103A-3	J103B-3	J103C-3	J103D-3	[illegible] / BLK	
C1-34	J103A-4	J103B-4	J103C-4	J103D-4	[illegible] / RED	
C1-41	J103A-1	J103B-1	J103C-1	J103D-1	[illegible] / GRN	TWISTED PAIR
C1-42	J103A-2	J103B-2	J103C-2	J103D-2	[illegible] / WHT	

CBL1284-001
CBL1284-002
CBL1284-003



VIEW A-A

NOTES:

1. STAMP MARKINGS "C1, J103", J103B, J103C, & J103D .10 HIGH IN WHITE INK. LOCATE APPROX. AS SHOWN.
2. STAMP NUMBERS 1 & 35 OVER END CONTACTS ON ITEMS "3 AS SHOWN IN VIEW A-A. STAMP NUMBERS "2 & "36 OVER END CONTACTS ON OPPOSITE SIDE OF ITEMS "3. NUMBERS TO BE .12 HIGH IN WHITE INK.
3. INSERT KEY (ITEM "17) BETWEEN SLOTS 5/16 & 7/16 OF ITEM "2.
4. INSERT KEY BETWEEN SLOTS 5/16 & 7/16 OF ITEMS "3
5. TYPE PART NUMBER & REVISION ON ITEM "15 AS SHOWN.
6. ALL UNUSED WIRES SEE TO BE TERMINATED INSIDE CABLE. (CUT OFF AT BOTH ENDS)
7. SEE DWN INSTRUCTIONS FOR CABLE CODING INSTRUCTIONS.

NO. OF TRANSPORTS PER CABLE

4	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
3	[illegible]	[illegible]	[illegible]	[illegible]	--
2	[illegible]	[illegible]	[illegible]	—	--

MATERIAL: SEE BOM

DRN: [illegible] 7/1/74

CHK: 1 7/1/74

PRIME COMPUTER, INC.
NATICK, MASS.

CABLE, DAISY CHAIN - MFC-2, TO PERTEC 7 & 9 TRACK MTT READ DATA CONN. E

SIZE D | CBL1284-XXX | REV E

PRIME COMPUTER INC.
NATICK MASS.

DWN. JHB 9/9/74 · CHK. J.C.T. 10/9/74 · ENG. J. Gevlin 10/10/74 · APPRD. HGM 10-9-74

STANDARD COST ______ DATE ______

TITLE: MAG TAPE CONTROLLER SUB ASSY EV

BOM MEC2043-XXX · REV. B1 · NHA: 4020-002 · SHT. 1 OF 3

REV.	ECN	CK
A	REL	—
B	1533	JBM

ITEM	SIZE	PART NUMBER	-001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1	D	MEC 1849-001	REF.								P.C. BOARD ETCH CUTS	
2	C	MEC 0537	1								STIFFENER ASSY, P.C. BOARD	
3		MEC 0303-005	5								SCREW, BD HD, CRES #4-40X 1/4 LG	
4		MEC 0356	5								WASHER, FLAT FIBER NO. 4	
5		MEC 0388-001	5								NUT, MINIATURE HEX #4-40	
6		CON 0650-001	24								SOCKET, 16 PIN (LOW PROFILE)	
7		WIR 1221-003	A/R								WIRE, BUS 22 AWG	
8		WIR 1365-004	A/R								WIRE, 30 AWG (YEL)	
9		WIR 1365-009	A/R								WIRE, 30 AWG (WHT)	
10		WIR 1365-002	A/R								WIRE, 30 AWG (RED)	
11		WIR 0653-000	A/R								WIRE, 24 AWG SINGLE COND (BLK)	
12		CAP 0129	152								CAP, CERAMIC DISC .01μF 25V	
13	B	MEC 1406-001	13								INSULATED BUS BAR	
14												
15		RES 0250-153	1								RESISTOR DIP 15KΩ	
16		RES 0250-471	5								RESISTOR DIP 470Ω	
17		RES 0667-003	4								RESISTOR DIP 220/330Ω	
18		RES 0221-550	5								RESISTOR 15K, 1/4W R3,4,5,6,7	
19		RES 0221-400	8								RESISTOR 2K, 1/4W R1,20,21,30 R89-92	
20		RES 0221-300	13								RESISTOR 470Ω, 1/4W R2, R33-39 R86,87,88,93,94	
21		CAP 0552-315	2								CAPACITOR, TANT 3.3μF 15V C1,2	
22		PCB 1601-001	1								P.C. BD. MPC-2 E.V.	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. JHB 9/9/74 · CHK. · ENG. · APPRD.

STANDARD COST ______ DATE ______

TITLE: MAG TAPE CONTROLLER SUB ASSY

BOM MEC2043-XXX · REV. B1 · NHA: · SHT. 3 OF 3

ITEM	SIZE	PART NUMBER	-001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
45		ICD 0057	1								74194	
46		ICD 0058	6								7442	
47		ICD 0059	1								8094	
48		ICD 0060	6								8262	
49		ICD 0070	1								74S64	
50		ICD 0071	1								74S74	
51		ICD 0072	5								74S112	
52		ICD 0076	3								74S174	
53		ICD 0078	1								74S194	
54		ICD 0085	1								74S00	
55		ICD 0086	2								74S04	
56		ICD 0088	1								74S10	
57		ICD 0089	3								74S11	
58		ICD 0106	6								7416	
59		ICD 0112	7								8095	
60		ICD 0186	2								74154	
61		ICD 0201	1								7474	
62		ICD 0664	1								7414	
63		ICD 0665	4								82S21	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. JHB 9/9/74 · CHK. · ENG. · APPRD.

STANDARD COST ______ DATE ______

TITLE: MAG TAPE CONTROLLER SUB ASSY

BOM MEC2043-XXX · REV. B1 · NHA: · SHT. 2 OF 3

ITEM	SIZE	PART NUMBER	-001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
23												
24		XTL 0654	1								OSCILLATOR	
25		ICD 0025	8								74H00	
26		ICD 0026	1								74H01	
27		ICD 0028	18								74H04	
28		ICD 0029	8								74H08	
29		ICD 0030	3								74H10	
30		ICD 0031	3								74H11	
31		ICD 0033	2								74H20	
32		ICD 0034	2								74H21	
33		ICD 0035	1								74H30	
34		ICD 0038	2								74H50	
35		ICD 0040	1								74H53	
36		ICD 0043	9								74H74	
37		ICD 0046	4								74H106	
38		ICD 0048	31								74151	
39		ICD 0049	6								74153	
40		ICD 0051	9								74157	
41		ICD 0052	10								74161	
42		ICD 0053	17								74174	
43		ICD 0054	17								74175	
44		ICD 0055	2								74181	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. JHB 9/16/74 · CHK. J.C.T. 9/19/74 · ENG. Gevlin 10/10/74 · APPRD. HGM 10-9-74

STANDARD COST ______ DATE ______

TITLE: CONTROLLER ASSY MAG TAPE EV

BOM 4020-XXX · REV. B · NHA: · SHT. 1 OF 1

REV.	ECN	CK
A	REL	—
B	1533	JBM

ITEM	SIZE	PART NUMBER	-001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1	D	MEC 2043-001	—	1							MAG TAPE CONTROLLER SUB ASSY	
2	A	MEC 1901-018	—	1							PROM SET (MAGICT)	
	A	SPC 1409	—	REF							SPEC, PRODUCT MPC-2	
	A	SPC 0642	—	REF							SPEC, PRODUCT MAG TAPE	
	C	LBD 1829	—	EV							LOGIC BLOCK DIAG MPC2 EV	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. JCR 7/24/73
CHK. JSN 1/10/75
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: CABLE, MAGNETIC TAPE CONTROLLER (CONTROL)
CONN. D

BOM CBL0659-XXX REV. D
NHA: 4141/4143 SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	R	JCR			
B	1206	JCR			
C	1210	JKB			
D	1520	JCR			

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1.		WIR1420	4'6"	12'6"	30'6"						CABLE, 22 T.P. 28AWG COLOR CODED	△
2.	B	CON0019	1	1	1						CONN. HOUSING C1	
3		CON0658	1	1	1						CONN HOUSING J1	
* 4		CON0163	65	65	65						CONTACTS, CRIMP	
5	B	MEC1236-001	1	1	1						BRACKET, CABLE CLAMP	
6	B	MEC1236-003	1	1	1						BRACKET, CABLE CLAMP	△
7	B	MEC1237-001	2	2	2						BLOCK, CABLE CLAMP	
8	A	MEC0311-002	2	2	2						SCREW, CAPTIVE	△
9		MEC0407-001	4	4	4						EYELET, FLAT FLANGE	△
10		CON0210	2	2	2						KEY, POLARIZING	
11		MEC0420	AS REQ	AS REQ	A/R						TAPE, DOUBLE COATED	△
12	A	MEC0311-001	2	2	2						SCREW, CAPTIVE	△ △
13	A	MEC 0421	1	1	1						MARKER, CABLE	△
	B	INS1210	REF	REF	REF						CABLE CODING LOCATION	
	*	0000002									TOOL, EXTRACTION	
	*	0000003									TOOL, CRIMPING	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. JCR 7/24/73
CHK. JSN 1/10/75
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: CABLE, MAGNETIC TAPE CONTROLLER (READ DATA)
CONN. E

BOM CBL0661-XXX REV. D
NHA: 4141/4143 SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	R	JCR			
B	1206	JCR			
C	1210	JKB			
D	1520	JCR			

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1.		WIR1420	4'6"	12'6"	30'6"						CABLE, 22 T.P. 28AWG COLOR CODED	△
2.	B	CON0019	1	1	1						CONN. HOUSING C1	
3		CON0658	1	1	1						CONN HOUSING J3	
* 4		CON0163	40	40	40						CONTACTS, CRIMP	
5	B	MEC1236-001	1	1	1						BRACKET, CABLE CLAMP	
6	B	MEC1236-003	1	1	1						BRACKET, CABLE CLAMP	△
7	B	MEC1237-001	2	2	2						BLOCK, CABLE CLAMP	
8	A	MEC0311-002	2	2	2						SCREW, CAPTIVE	△
9		MEC0407-001	4	4	4						EYELET, FLAT FLANGE	△
10		CON0210	2	2	2						KEY, POLARIZING	
11		MEC0420	AS REQ	AS REQ	A/R						TAPE, DOUBLE COATED	△
12	A	MEC0311-001	2	2	2						SCREW, CAPTIVE	△ △
13	A	MEC 0421	1	1	1						MARKER, CABLE	△
	B	INS1210	REF	REF	REF						CABLE CODING INSTRUCTIONS	
	*	0000002									TOOL, EXTRACTION	
	*	0000003									TOOL, CRIMPING	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. JCR 1/24/73
CHK. JSN 1/10/75
ENG.
APPRD.
STANDARD COST _____ DATE _____

TITLE: CABLE, MAGNETIC TAPE CONTROLLER (WRITE DATA)
CONN. C

BOM CBL0660-XXX REV. C
NHA: 4141/4143 SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	R	JCR			
B	1206	JCR			
C	1210	JKB			
D	1520	JCR			

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1.		WIR1420	4'6"	12'6"	30'6"						CABLE, 22 T.P. 28 AWG COLOR CODED	△
2.	B	CON0019	1	1	1						CONN. HOUSING C1	
3		CON0658	1	1	1						CONN HOUSING J2	
* 4		CON0163	48	48	48						CONTACTS, CRIMP	
5	B	MEC1236-001	1	1	1						BRACKET, CABLE CLAMP	
6	B	MEC1236-003	1	1	1						BRACKET, CABLE CLAMP	△
7	B	MEC1237-001	2	2	2						BLOCK, CABLE CLAMP	
8	A	MEC0311-002	2	2	2						SCREW, CAPTIVE	△
9		MEC0407-001	4	4	4						EYELET, FLAT FLANGE	△
10		CON0210	2	2	2						KEY, POLARIZING	
11		MEC0420	AS REQ	AS REQ	A/R						TAPE, DOUBLE COATED	△
12	A	MEC0311-001	2	2	2						SCREW, CAPTIVE	△ △
13	A	MEC 0421	1	1	1						MARKER, CABLE	△
	B	INS1210	REF	REF	REF						CABLE CODING LOCATION	
	*	0000002									TOOL, EXTRACTION	
	*	0000003									TOOL, CRIMPING	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. J.C.R
CHK. J.B 9/27/73
ENG. D. Gardner
APPRD.
STANDARD COST _____ DATE _____

TITLE: CABLE, DAISY CHAIN
MAGNETIC TAPE TRANSPORT
CONTROL CONN. D.
PERTEC 7 & 9 TRACK

BOM CBL1282-XXX REV. E
NHA: 4141/4143 SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	RELEASED	J.C.R	E	1520	JPL
B	1211	JAB			
C	1374	JCR			
D	1486	JCR			

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1.		WIR1420	21'	29'	30'						WIRE, 22 T.P. 28AWG COLOR CODED.	△
2	B	CON0019	1	1	1						CONNECTOR HOUSING, 44 POS. C1	
3		CON0658	2	3	4						CONNECTOR HOUSING, 36 POS. J1, J101	
4		CON0163	64	64	64						CONTACTS, CRIMP (28-24)	△
5		CON0251	31	62	93						CONTACTS, CRIMP (24-20).	
6	B	MEC1236-001	1	1	1						BRACKET, CABLE CLAMP	
7	B	MEC1236-003	2	3	4						BRACKET, CABLE CLAMP	
8	B	MEC1237-001	3	4	5						BLOCK, CABLE CLAMP	
9		MEC0420	AS REQ	AS REQ	AS REQ						TAPE, DOUBLE COATED	
10		CON0210	3	4	5						KEY, POLARIZING	
11		MEC0182-002	4	6	8						CABLE TIE	△
12	A	MEC0311-002	4	6	8						SCREW, CAPTIVE	
13		MEC0407-001	6	8	10						EYELET, FLAT FLANGE	△
14	A	MEC0311-001	2	2	2						SCREW, CAPTIVE	
15	A	MEC0421	1	1	1						MARKER, CABLE	
16		WIR0542-002	AS REQ	AS REQ	AS REQ						WIRE, #22 AWG STRANDED RED	△

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PRIME COMPUTER INC.
NATICK MASS.

DWN. J.C.R
CHK. J.B 9/27/73
ENG. D. Gardner
APPRD.
STANDARD COST _____ DATE _____

TITLE: CABLE, DAISY CHAIN
MAG. TAPE TRANSPORT
READ DATA CONN. E
PERTEC 7 & 9 TRACK

BOM CBL1284-XXX REV. E
NHA: 4141/4143 SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	RELEASED	J.C.R	E	1520	JPL
B	1211	JAB			
C	1374	JCR			
D	1486	JCR			

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1.		WIR1420	21'	29'	30'						WIRE, 22 T.P. 28AWG COLOR CODED	△△
2	B	CON0019	1	1	1						CONNECTOR HOUSING, 44 POS. C1	
3		CON0658	2	3	4						CONNECTOR HOUSING, 36 POS. J103A J103B J103C, J103B	△
4		CON0163	40	40	40						CONTACTS, CRIMP (28-24)	
5		CON0251	20	40	60						CONTACTS, CRIMP (24-20).	
6	B	MEC1236-001	1	1	1						BRACKET, CABLE CLAMP	
7	B	MEC1236-003	2	3	4						BRACKET, CABLE CLAMP	
8	B	MEC1237-001	3	4	5						BLOCK, CABLE CLAMP	
9		MEC0420	AS REQ	AS REQ	AS REQ						TAPE, DOUBLE COATED	
10		CON0210	3	4	5						KEY, POLARIZING	
11		MEC0182-002	4	6	8						CABLE TIE	△
12	A	MEC0311-002	6	8	10						SCREW, CAPTIVE	
13		MEC0407-001	6	8	10						EYELET, FLAT FLANGE	△
14	A	MEC0311-001	2	2	2						SCREW, CAPTIVE	
15	A	MEC0421	1	1	1						MARKER, CABLE	

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PRIME COMPUTER INC.
NATICK MASS.

DWN. J.C.R
CHK. J.B 9/27/73
ENG. D. Gardner
APPRD.
STANDARD COST _____ DATE _____

TITLE: CABLE, DAISY CHAIN
MAGNETIC TAPE TRANSPORT
WRITE DATA CONN. C.
PERTEC 7 & 9 TRACK

BOM CBL1283-XXX REV. C
NHA: 4141/4143 SHT. 1 OF 1

REV.	ECN	CK	REV.	ECN	CK
A	RELEASED	J.C.R			
B	1374	JCR			
C	1486	JCR			

ITEM	SIZE	PART NUMBER	QUANTITY -001	-002	-003	-004	-005	-006	-007	-008	DESCRIPTION	STANDARD COST
1.		WIR1420	21'	29'	30'						WIRE, 22 T.P. 28 AWG COLOR CODED	△△
2	B	CON0019	1	1	1						CONNECTOR HOUSING, 44 POS. C1	
3		CON0658	2	3	4						CONNECTOR HOUSING, 36 POS. J102C J102A, J102B J102D	△
4		CON0163	48	48	48						CONTACTS, CRIMP (28-24)	
5		CON0251	24	48	72						CONTACTS, CRIMP (24-20).	
6	B	MEC1236-001	1	1	1						BRACKET, CABLE CLAMP	
7	B	MEC1236-003	2	3	4						BRACKET, CABLE CLAMP	
8	B	MEC1237-001	3	4	5						BLOCK, CABLE CLAMP	
9		MEC0420	AS REQ	AS REQ	AS REQ						TAPE, DOUBLE COATED	
10		CON0210	3	4	5						KEY, POLARIZING	
11		MEC0182-002	4	6	8						CABLE TIE	
12	A	MEC0311-002	4	6	8						SCREW, CAPTIVE	△
13		MEC0407-001	6	8	10						EYELET, FLAT FLANGE	△
14	A	MEC0311-001	2	2	2						SCREW, CAPTIVE	
15	A	MEC0421	1	1	1						MARKER, CABLE	

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